Architecture of Microprocessor – 8085

- **Instruction Register**
  - It is an 8- bit register.
  - It contains the 8- bit Opcode of a particular instruction.
- **Instruction Decoder and Machine Cycle Encoder**

  This unit decodes the instruction stored in the instruction register.

  It determines the nature of instruction establishes the sequence of events to be followed by the timing and control unit.
- **General Purpose Register**

  There are Six 8- bit general purpose registers namely B, C, D, E, H and L registers.

Special Purpose Registers

There are two special purpose registers such as

- Stack Pointer (SP)
- Program Counter (PC)

Stack Pointer (SP)

- It is a 16- bit register.
- It will hold the address of the stack memory.

Program Counter (PC)

- It is a 16- bit register.
- This register will hold the starting address of programs and when one instruction is fetched from memory, PC is automatically incremented to point out the address of next instruction.

Increment/ Decrement Address Latch

- This 16- bit register is used to increment/ decrement the content of PC or SP as a part of execution of instructions related to them.

Timing and Control Unit

The internal clock generator is available in this unit.

Power Supply Pins

V_{CC} & GND these two pins are Power Supply Pins for µp 8085.

Clock Signals

X_1 & X_2 and CLK OUT are used as a clock signals.

Control Signals

Control Signals are **RD & WR**

ALE

ALE is Address Latch Enable.

This signal is used to enable the latch.

This signal is used for demultiplexing of multiplexing buses.

Status Signals

These signals are IO/ $\overline{M}$, S_0 and S_1.

$\overline{\text{RESET IN}}$

This signal is used to reset the µp.

RESET OUT

This signal is used to reset all the connected devices when the µp is reset.

- **READY**

  This signal indicates that the device is ready to send or receive data.

  If READY is low, then the CPU has to wait for READY to go high.

- **DMA Signals**

  Two signals are used to request and acknowledge a direct memory access (DMA) transfer in a microprocessor-based system.

- **HOLD**

  It is used to request a DMA action.

- **HLDA**

  Signal as an output that acknowledge the DMA action.

Interrupt Control

Interrupts are the signals generated by external devices to request the microprocessor to perform a task.

There are 5 interrupt signals

- TRAP
- RST7.5
- RST6.5
- RST5.5
- INTR

- **$\overline{\text{INTA}}$** It is an interrupt acknowledgement sent by the microprocessor after INTR is received.

Serial I/O Control

- These signals are used for serial communication.
- SOD (Serial Output Data line)
- The output SOD is Set/Reset as specified by the SIM instruction.
- SID (Serial Input Data line)
- The data on this line is loaded into accumulator whenever RIM instruction is executed.

Address Buffer and Address/ Data Buffer

- The Higher Address bus is an 8- bit unidirectional bus from which the higher order address bits $A_8 - A_{15}$ are transferred from the microprocessor to the memory and peripherals.
- The Lower Address/Data bus is an 8- bit bidirectional bus used for sending lower order address bits $A_0 - A_7$ and sending and receiving the data bits $D_0 - D_7$ to the memory and peripherals.
- The Lower Address and Data Bus are Multiplexed Bus.
- These Pins are also Time Sharing Pins.
- During the First CLK Pulse Lower 8-bit Address is transferred.
- During the Second and Third CLK Pulse same Pins are used for Data transfer.

Program Status Word

- It is an 8- bit register but only five bits are used.
- It is also called Flag Register.

S	Z	X	AC	X	P	X	CY

Program Status Word

- **S** Sine Flag
- **Z** Zero Flag
- **AC** Auxiliary Carry Flag
- **P** Parity Flag
- **CY** Carry Flag.

The status of different Flags are given in the following table

Flags	Value	Comments
Carry Flag	0	When carry is not generated.
Carry Flag	1	When carry is generated.
Parity Flag	0	When no. of 1's is odd.
Parity Flag	1	When no. of 1's is even.
Auxiliary Carry Flag	0	When carry is not generated after addition of 4 bits in an 8-bit number.
Auxiliary Carry Flag	1	When carry is generated after addition of 4 bits in an 8-bit no.
Zero Flag	0	When result is non- zero number.
Zero Flag	1	When result is a zero number.
Sign Flag	0	When MSB is equal to 0.
Sign Flag	1	When MSB is equal to 1.

Control Signals

- There are Two Control signals
  - $\overline{RD}$ & $\overline{WR}$
  - These signals are active Low.
  - These signals are valid only for one CLK Pulse

IO/$\overline{M}$	$\overline{RD}$	$\overline{WR}$	Operation
0	0	1	MEMR
0	1	0	MEMW
1	0	1	IOR
1	1	0	IOW

Status Signals

- There are Three Status Signal
  - $IO/\overline{M}$, S1,S0
  - $IO/\overline{M}$ = 0 ie; Memory is selected
  - $IO/\overline{M}$ = 1 ie; Memory is not selected. I/O Device is selected
  - S1 and S0 are give the status of Machine Cycle.

$IO/\overline{M}$	S1	S0	Machine Cycle
0	1	0	MEMR(3T)
0	0	1	MEMW(3T)
1	1	0	IOR(3T)
1	0	1	IOW(3T)
0	1	1	Opcode Fetch(4T)