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MOS INVERTER

(CMOS INVERTER)

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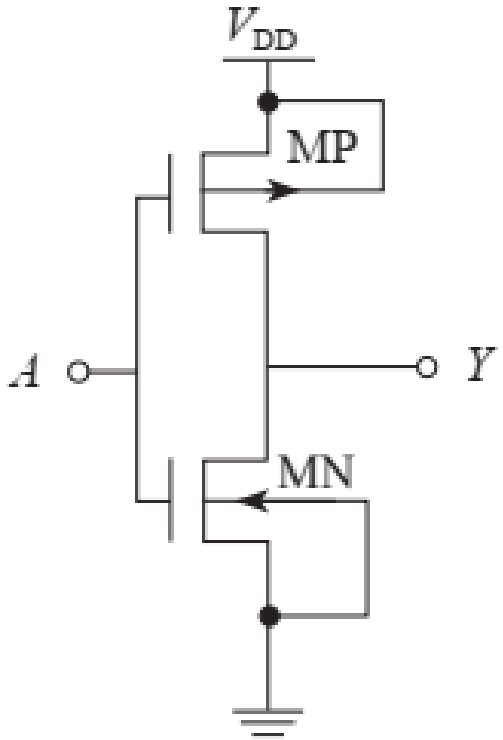
CMOS Inverter

- Complementary MOS (CMOS) Inverter uses
  - pMOS in pull-up network
  - nMOS in pull-down network

  As shown in Figure
- When input is HIGH
  - pMOS is OFF
  - nMOS is ON
  - Therefore the O/P is LOW
- When input low
  - pMOS is ON
  - nMOS is OFF
  - Therefore the O/P is HIGH



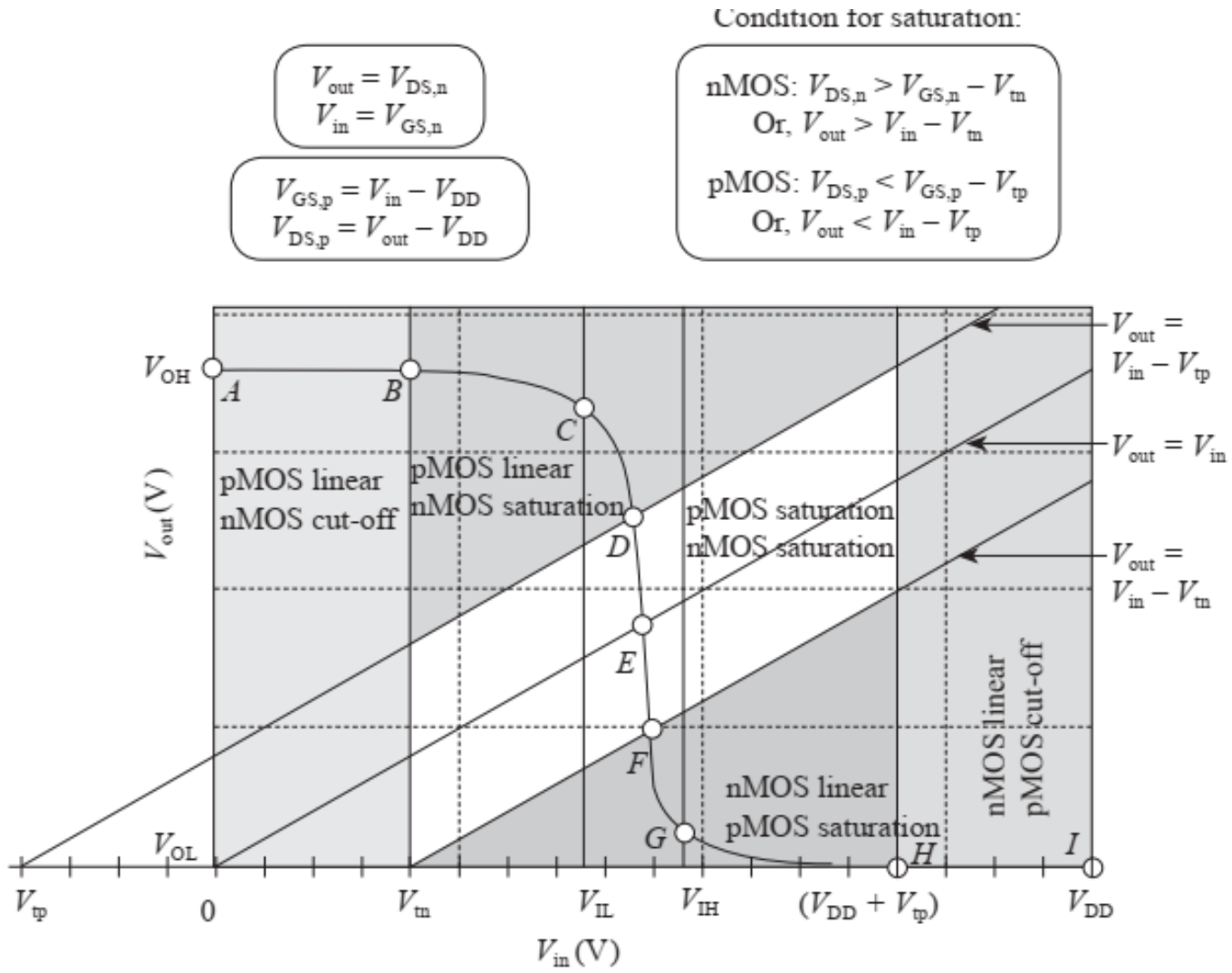
CMOS Inverter

- Advantage of CMOS Inverter
  - Never pMOS and nMOS are ON together due to which there is no direct path to current take place between V_{DD} and ground.
  - Therefore if we neglect leakage current, the static power dissipation is zero.
  - Logic swing is between o and V_{DD}.

Voltage Transfer Characteristics

- VTC is shown in fig which is divided into five regions depending on the operation of nMOS and pMOS.
- In between pt A and B
  - nMOS in cutoff region
  - pMOS in linear region
- In between pt B and C
  - nMOS in saturation region
  - pMOS in linear region

Voltage Transfer Characteristics



Voltage Transfer Characteristics

$$V_{out} = V_{in} - V_{tp},$$

- Region above this line ,pMOS operates in linear region.
- Below this line, pMOS operates in saturation region with satisfying the condition

$$V_{DS} \leq V_{GS} - V_{tp} \text{ or } V_{out} \leq V_{in} - V_{tp}$$

- At point C,Slope is -1, this is V_{IL}
- Between D and F,
  - both the nMOS and pMOS are in saturation region.

Voltage Transfer Characteristics

- At C,
  - I/P voltage = O/P voltage
  - which is also called threshold voltage of the inverter.
- Between F and H,
  - nMOS in the linear region and
  - pMOS in the saturation region.
- At pt G, Slope is -1, known as $V_{IH.}$
- Between H and I,
  - nMOS is in the linear region and
  - pMOS in the cutoff region.

Voltage Transfer Charateristics

$$V_{out} = V_{in} - V_{tn}$$

- Above this line nMOS in saturation and satisfies the condition

$$V_{DS} \geq V_{GS} - V_{tn} \text{ or, } V_{out} \geq V_{in} - V_{tn}$$

- Below this line,nMOS works in linear region.

We observe that the VTC curve of a CMOS inverter is very sharp compared to the resistive load and nMOS load inverter circuits.

Calculation of V_{IL}

- In between pt B and D
  - nMOS in saturation region
  - pMOS in linear region

  Therefore we have the following equation

$$\frac{\beta_n}{2}(V_{GS,n} - V_{tn})^2 = \frac{\beta_p}{2}\left[2(V_{GS,p} - V_{tp})V_{DS,p} - V_{DS,p}^2\right]$$

$$\frac{\beta_n}{2}(V_{in} - V_{tn})^2 = \frac{\beta_p}{2}\left[2(V_{in} - V_{DD} - V_{tp})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2\right]$$

Calculation of V_{IL}

- Differentiating w.r.t. Vin

$$\beta_n (V_{in} - V_{tn}) =$$

$$\beta_p \left[(V_{out} - V_{DD}) + (V_{in} - V_{DD} - V_{tp}) \left(\frac{dV_{out}}{dV_{in}} \right) - (V_{out} - V_{DD}) \left(\frac{dV_{out}}{dV_{in}} \right) \right]$$

- At point C, the slope of the curve is -1 and *V*in= *V*IL. Therefore, we write above Eqn as follows:

$$\beta_n (V_{IL} - V_{tn}) = \beta_p [(V_{out} - V_{DD}) - (V_{IL} - V_{DD} - V_{tp}) + (V_{out} - V_{DD})]$$

Calculation of V_{IL}

$$\beta_n (V_{IL} - V_{tn}) = \beta_p [2V_{out} - V_{DD} - V_{IL} + V_{tp}]$$

$$\left(\frac{\beta_n}{\beta_p} + 1 \right) V_{IL} = 2V_{out} - V_{DD} + V_{tp} + \frac{\beta_n}{\beta_p} V_{tn}$$

$$V_{IL} = \frac{2V_{out} - V_{DD} + V_{tp} + \frac{\beta_n}{\beta_p} V_{tn}}{\left(\frac{\beta_n}{\beta_p} + 1 \right)}$$

Calculation of V_{IH}

- Between F and H,
  - nMOS in the linear region and
  - pMOS in the saturation region

Therefore we have the following equation

$$\frac{\beta_n}{2}[2(V_{GS,n}-V_{tn})V_{DS,n}-V_{DS,n}^2]=\frac{\beta_p}{2}(V_{GS,p}-V_{tp})^2$$

$$\frac{\beta_n}{2}[2(V_{in}-V_{tn})V_{out}-V_{out}^2]=\frac{\beta_p}{2}(V_{in}-V_{DD}-V_{tp})^2$$

Calculation of V_{IH}

- Differentiating w.r.t. Vin, $$\beta_n\left[V_{out}+(V_{in}-V_{tn})\left(\frac{dV_{out}}{dV_{in}}\right)-V_{out}\left(\frac{dV_{out}}{dV_{in}}\right)\right]=\beta_p(V_{in}-V_{DD}-V_{tp})$$

- At point G, the slope of the curve is -1 and *V*in= V_{IH}.

  Therefore, we write above Eqn as follows:

$$\beta_n(2V_{out}-V_{IH}+V_{tn})=\beta_p(V_{IH}-V_{DD}-V_{tp})$$

$$\left(\frac{\beta_n}{\beta_p}+1\right)V_{IH}=V_{DD}+V_{tp}+\frac{\beta_n}{\beta_p}(2V_{out}+V_{tn})$$

$$V_{IH}=\frac{V_{DD}+V_{tp}+\frac{\beta_n}{\beta_p}(2V_{out}+V_{tn})}{\frac{\beta_n}{\beta_p}+1}$$

Calculation of V_{OL}

- O/P of CMOS Inverter is given by

$$V_{out} = V_{DS,n}$$

- I/P= logic '1' (i.e., *V*in > *V*DD + *V*tp),
  - the pMOS transistor is turned OFF, and
  - the nMOS transistor operates in the linear region.
  - Since there is no static current in the circuit, there is no voltage drop across the nMOS transistor.

Calculation of V_{OL}

- Therefore, we have the following expression:

$$I_{D,n} = \frac{\beta_n}{2}[2(V_{GS,n} - V_{tn})V_{DS,n} - V_{DS,n}^2] = 0$$

$$2(V_{GS,n} - V_{tn})V_{DS,n} - V_{DS,n}^2 = 0$$

- By solving, we get

$$(2V_{GS,n} - 2V_{tn} - V_{DS,n})V_{DS,n} = 0$$

$$V_{DS,n} = 0$$

- O/P voltage

$$V_{out} = V_{OL} = 0$$

Calculation of V_{OH}

- I/P=o (i.e., *V*in < *V*tn),
  - the nMOS transistor is turned OFF,and
  - the pMOS transistor operates in the linear region. As there is no static current in the circuit, there is no voltage drop across the pMOS transistor.

  Hence, the output voltage is given by the following equation:

$$V_{out} = V_{OH} = V_{DD}$$

Calculation of V_{th}

- Threshold voltage when I/P voltage=O/P voltage $V_{th} = V_{in} = V_{out}$
- On VTC,Vth is defined at E, when nMOS and pMOS both operates in saturation region
- Therefore, we can write following equation

$$\frac{\beta_n}{2}(V_{GS,n} - V_{tn})^2 = \frac{\beta_p}{2}(V_{GS,p} - V_{tp})^2$$

$$\sqrt{\frac{\beta_n}{\beta_p}}(V_{in} - V_{tn}) = \pm(V_{in} - V_{DD} - V_{tp})$$

$$V_{th} = \frac{V_{tn}\sqrt{\frac{\beta_n}{\beta_p}} + V_{DD} + V_{tp}}{\sqrt{\frac{\beta_n}{\beta_p}} + 1}$$

Example

Calculate the critical voltages and noise margins for a CMOS inverter, given the following values:

$$V_{DD} = 5.0\ \text{V},\ V_{tn} = 0.4\ \text{V},\ V_{tp} = -0.4\ \text{V},\ \beta_n = 50\ \mu\text{A/V}^2 \text{ and } \beta_p = 20\ \mu\text{A/V}^2$$

Solution

$$V_{IL} = \frac{2V_{out} - V_{DD} + V_{tp} + \dfrac{\beta_n}{\beta_p} V_{tn}}{\left(\dfrac{\beta_n}{\beta_p} + 1\right)}$$

$$= \frac{2V_{out} - 5.0 + (-0.4) + \dfrac{50}{20} \times 0.4}{\dfrac{50}{20} + 1}$$

$$= \frac{2V_{out} - 5.0 - 0.4 + 1.0}{2.5 + 1} = \frac{2V_{out} - 4.4}{3.5} = 0.57V_{out} - 1.26$$

Example

$$\frac{\beta_n}{2}(V_{in}-V_{tn})^2=\frac{\beta_p}{2}\left[2(V_{in}-V_{DD}-V_{tp})(V_{out}-V_{DD})-(V_{out}-V_{DD})^2\right]$$

$$\frac{50}{2}(0.57V_{out}-1.26-0.4)^2=$$

$$\frac{20}{2}[2(0.57V_{out}-1.26-5.0-(-0.4))(V_{out}-5.0)-(V_{out}-5.0)^2]$$

Or,

$$25(0.57V_{out}-1.66)^2=10[2(0.57V_{out}-5.86)(V_{out}-5.0)-(V_{out}^2-10V_{out}-25)]$$

Or,

$$25(0.3249V_{out}^2-1.8924V_{out}+2.7556)=$$

$$10[2(0.57V_{out}^2-2.85V_{out}-5.86V_{out}+29.3)-V_{out}^2+10V_{out}+25]$$

Example

Or,
$$8.1225V_{out}^2 - 47.31V_{out} + 68.89 - 11.4V_{out}^2 + 57V_{out}$$
$$+117.2V_{out} - 586 + 10V_{out}^2 - 10V_{out} - 25 = 0$$

Or,
$$6.7225V_{out}^2 + 116.89V_{out} - 542.11 = 0$$

Or,
$$V_{out}^2 + 17.388V_{out} - 80.64 = 0$$

Or,
$$V_{out} = \frac{-17.388 \pm \sqrt{302.34 + 322.56}}{2} = \frac{-17.388 \pm 24.998}{2}$$
$$= 3.805 \text{ V and } -28.193 \text{ V}$$

Example

- Positive value is acceptable for Vout
- Hence V_{IL} is calculated

$$V_{IL} = 0.57V_{out} - 1.26 = 0.57 \times 3.805 - 1.26 = 0.90885 \text{ V}$$

$$V_{IH} = \frac{V_{DD} + V_{tp} + \frac{\beta_n}{\beta_p}(2V_{out} + V_{tn})}{\frac{\beta_n}{\beta_p} + 1}$$

$$= \frac{5.0 + (-0.4) + \frac{50}{20}(2V_{out} + 0.4)}{\frac{50}{20} + 1}$$

$$= \frac{5.0 - 0.4 + 5V_{out} + 1.0}{2.5 + 1}$$

$$= \frac{5V_{out} + 5.6}{3.5} = 1.43V_{out} + 1.6$$

Example

$$\frac{\beta_n}{2}[2(V_{in}-V_{tn})V_{out}-V_{out}^2]=\frac{\beta_p}{2}(V_{in}-V_{DD}-V_{tp})^2$$

Or, $$\frac{50}{2}[2(1.43V_{out}-0.4)V_{out}-V_{out}^2]=\frac{20}{2}(1.43V_{out}+1.6-5.0-(-0.4))^2$$

Or, $$35.75V_{out}^2-10V_{out}-25V_{out}^2-10(2.0449V_{out}^2-8.58V_{out}+9)=0$$

Or, $$9.699V_{out}^2-75.8V_{out}+90=0$$

Or, $$V_{out}^2-7.815V_{out}+9.279=0$$

Or, $$V_{out}=\frac{7.815\pm\sqrt{61.074-37.116}}{2}=\frac{7.815\pm4.895}{2}=6.355\text{ V and }1.46\text{ V}$$

Example

The acceptable value of V_{out} is 1.46 V, as the other value (>power supply) is invalid. Therefore, V_{IH} can be calculated as follows:

$$V_{IH} = 1.43V_{out} + 1.6 = 1.43 \times 1.46 + 1.6 = 3.6878 \text{ V}$$

Therefore, the maximum value for logic '0' and minimum value of logic '1' of the output voltage are as follows:

$$V_{OL} = 0 \text{ and } V_{OH} = 5.0 \text{ V}$$

Using these values, the noise margins are calculated as follows:

$$\text{NM}_L = V_{IL} - V_{OL} = 0.90885 - 0 = 0.90885 \text{ V}$$

$$\text{NM}_H = V_{OH} - V_{IH} = 5 - 3.6878 = 1.3122 \text{ V}$$

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