DAC

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Introduction

The digital to analog converters compose the devices transforming a digital word, binary encoded and generated for example by a computer, into a discrete analog signal, in the sense that to every input digital word a single output analog value corresponds.

Weighted Resistor DAC

Weighted **Resistor D/A Converter**

The simplest D/A converter is obtained by means of a summing circuit with input resistances whose value depends on the bit weight that are associated to. We obtain in this way the weighted resistors converter whose diagram is shown in Fig.2 for the 4 bit case, where the switches $S_3 - S_0$ are driven from the digital information so that every resistance is connected to the reference

voltage V_{REF} or to ground in accordance with the fact that the corresponding bit is at logical level 1 or 0.

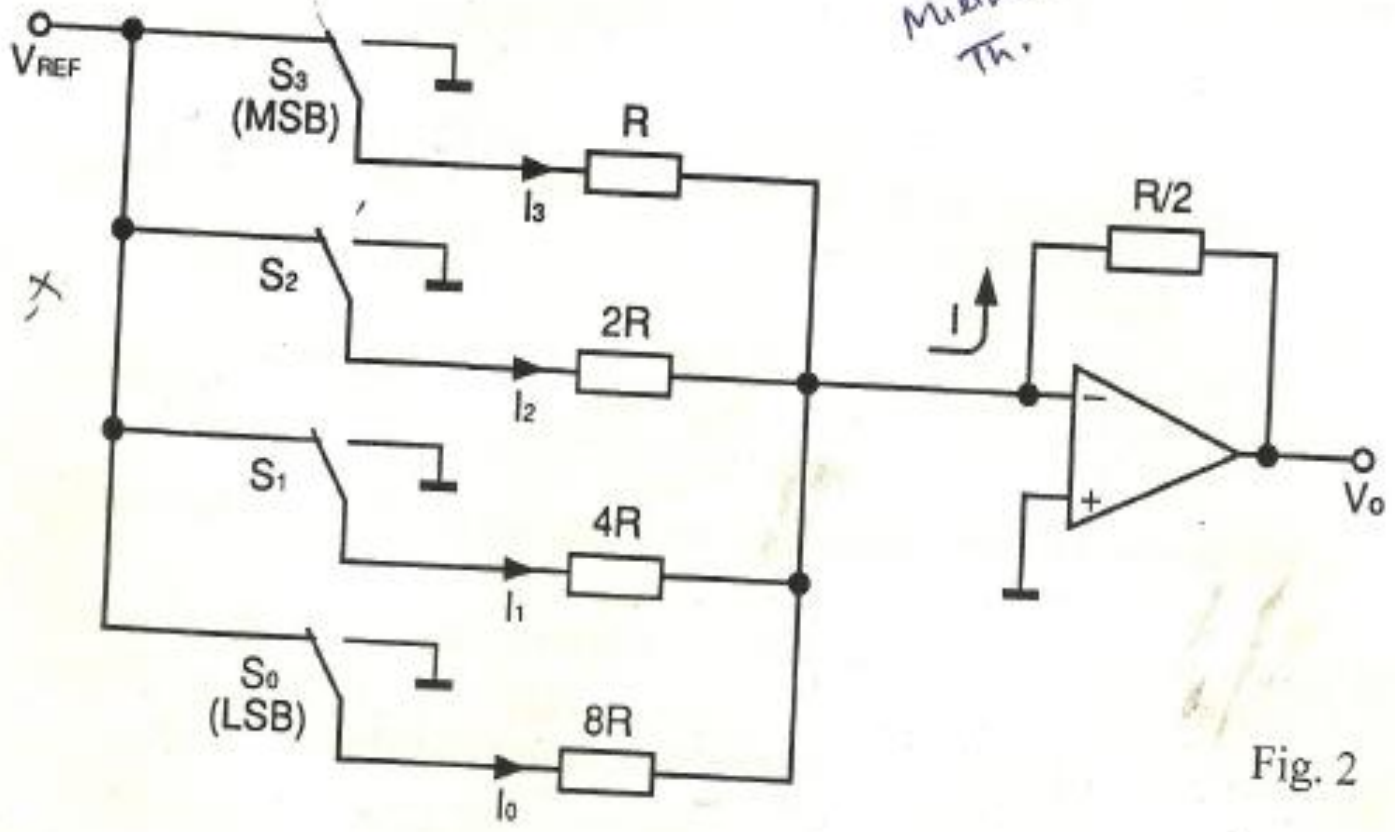


Fig. 2

Let's consider now the possibility where only the most significant bit (MSB) S_3 is at level 1: in the R resistance the current $I_3 = V_{REF} / R$ will flow and therefore at the operational amplifier output we will have the voltage

$$V_{o3} = -I_3 (R / 2) = - V_{REF} / 2$$

Analogously the contribution to the output voltage provided by the immediately less significant digit will result

$$V_{o2} = -I_2 (R / 2) = - (V_{REF} / 2R) (R / 2) = - V_{REF} / 4$$

and so on

$$V_{o1} = -I_1 (R / 2) = - (V_{REF} / 4R) (R /2) = - V_{REF} / 8$$

$$V_{o0} = I_0 (R / 2) = - (V_{REF} / 8R) (R / 2) = - V_{REF} / 16$$

The operational amplifier works as current to voltage converter, by summing the currents in the branches where the switch Si = 1, and it provides in output a voltage proportional to the total current and therefore to the binary value of the input signal :

$$V_o = -\frac{V_{REF}}{16}(8 \cdot S_3 + 4 \cdot S_2 + 2 \cdot S_1 + 1 \cdot S_0)$$

When all the bits are at logical level 1 the output voltage assumes the maximum full scale value

$$V_{OFS} = -0.9375\ V_{REF}$$

While the quantum, that represents the minimum increase of the output voltage in correspondence to the least significant bit (LSB) results

$$Q = -0.0625\ V_{REF}$$

The main disadvantage of this converter is that resistances of different value in a very wide field are demanded, above all at the increasing of the bit number, and therefore that can be carried out with limited accuracy.

R-2R Ladder DAC

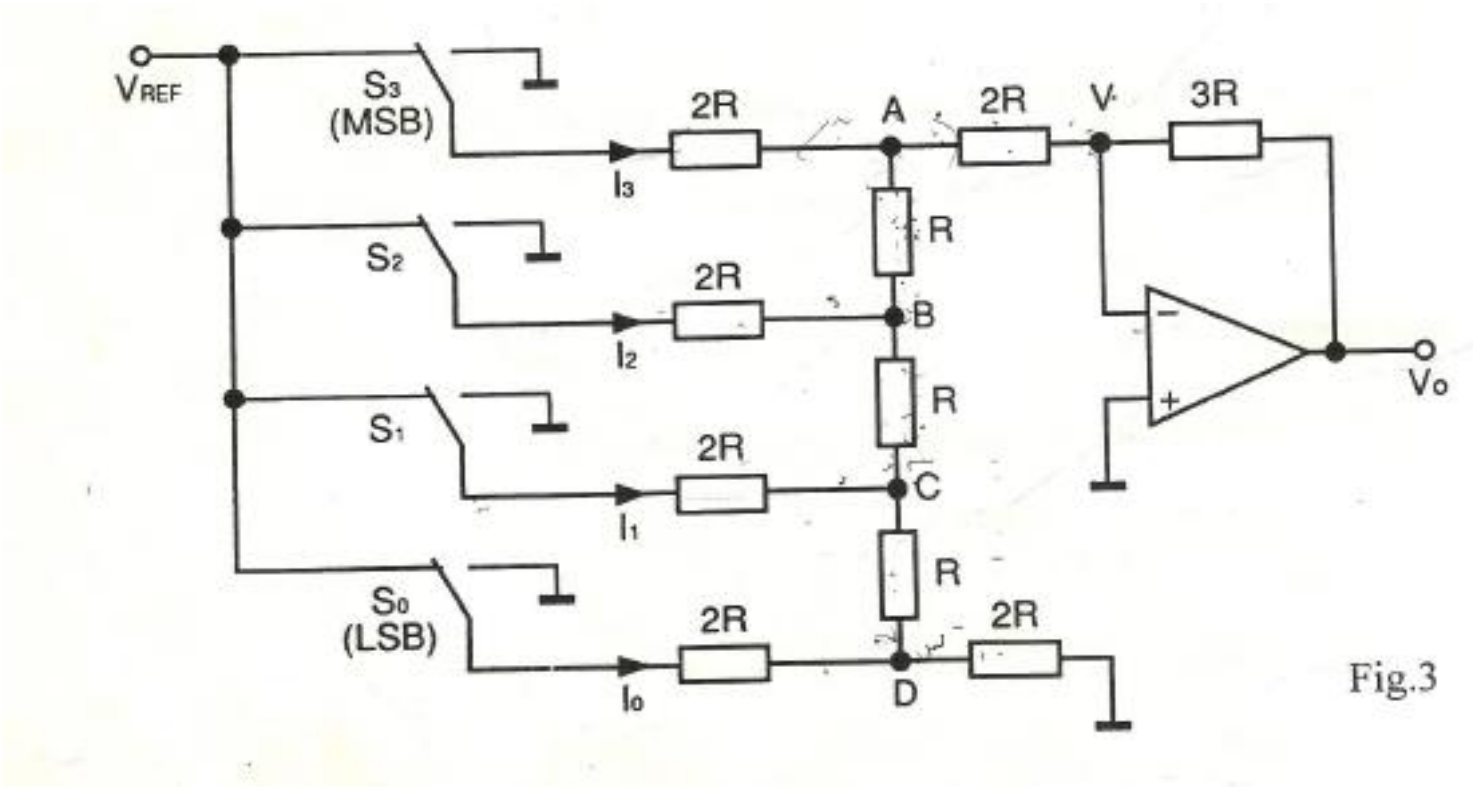
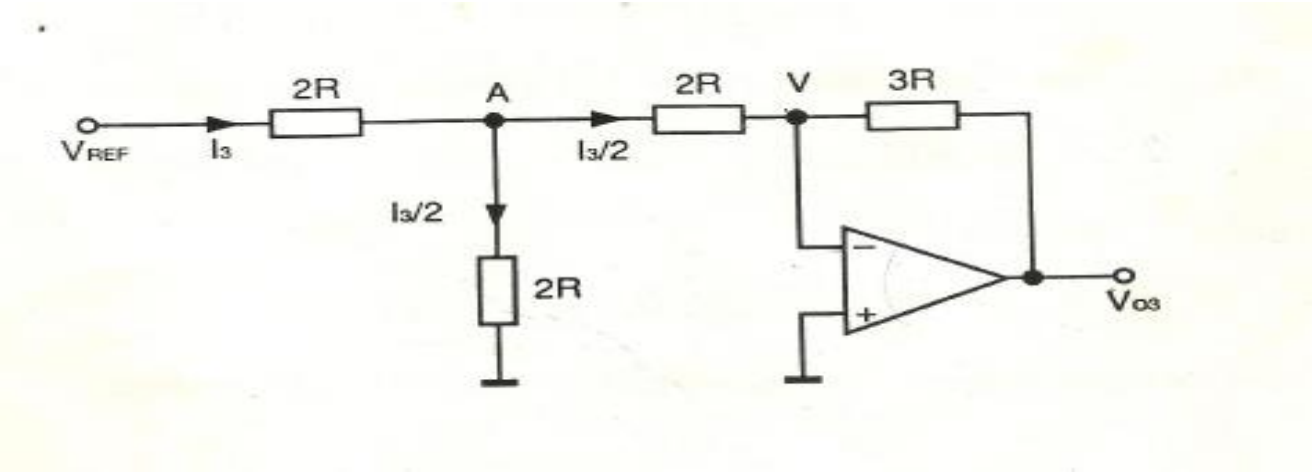


Fig.3

If we suppose at first that all the input bits are at low level ($S_3\ S_2\ S_1\ S_0 = 0000$) every switch grounds the respective resistance 2R : in these conditions, since point V is a virtual ground, the nodes A,B,C,D see toward ground, and in every direction, always the same resistance 2R.

Let's consider now the possibility where only the most significant bit S_3 is at level 1: the current I_3, delivered from the reference voltage V_{REF}, will divide in node A into two identical currents but equal to the half of the incoming one, as it is shown in Fig.4



Being

$$I_3 = V_{REF} / 2R+(2R//2R) = V_{REF}/ 3R$$

the potential of node A against ground is equal to

$$V_{A3} = 2R \cdot I_3 / 2 = (1 / 3) \cdot V_{REF}$$

and therefore at the operational amplifier output the voltage results

$$V_{03} = - 3R/ 2R \cdot (1 / 3) \cdot V_{REF} = - V_{REF} / 2$$

Analogously the contribution to the output voltage of the immediately less significant digit is determined by noticing that the current delivered from the reference voltage V_{REF} is equal to

$$I_2 = V_{REF} / 2R+(2R//2R) = V_{REF} / 3R = I_3$$

and it divides itself in node B into two identical currents of value $I_2/2$: this now current will split equally at node A so the potential of node A against ground is now equal to

$$V_{A2} = 2R \cdot (I_2 / 4) = (1/6) \cdot V_{REF}$$

and therefore at the operational amplifier output the voltage results

$$V_{02} = - 3R/2R. \ 1/6 \ V_{REF} = - V_{REF} / 4$$

with analog reasonings we obtain

$$I_1 = V_{REF}/3R$$

$$V_{A1} = 2R \cdot (I_1 / 8) = (1/12)\ V_{REF}$$

$$V_{o1} = -\ V_{REF} / 8$$

and at the end

$$I_0 = V_{REF} / 3R$$

$$V_{A0} = 2R(I_0 / 16) = (1/24)\ V_{REF}$$

$$V_{o0} = -\ V_{REF} / 16$$

By applying the principle of effect superposition the output voltage results at the end

$$V_o = -V_{REF}\,(8.S_3 + 4.S_2 + 2.S_1 + 1.S_0) / 16$$

When all the bits are at logic level 1 the output voltage assumes the maximum full scale value

$$V_{OFS} = -0.9375\ V_{REF}$$

While the quantum, that represents the minimum increase of the output voltage in correspondence of the least significant bit (LSB), results

$$Q = -0.0625\ V_{REF}$$