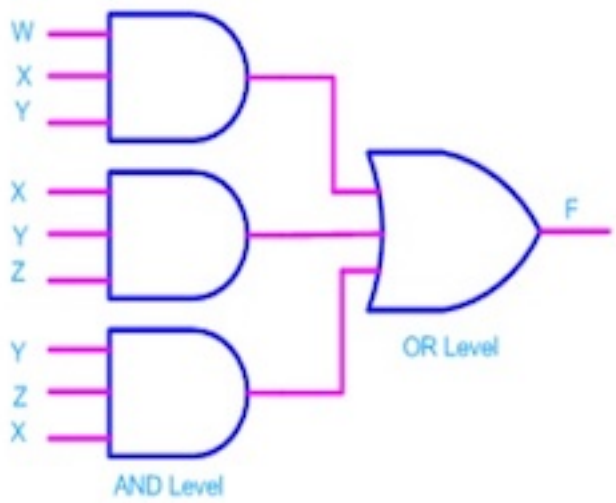
LECTURE-3

NAND AND NOR IMPLEMENTATION

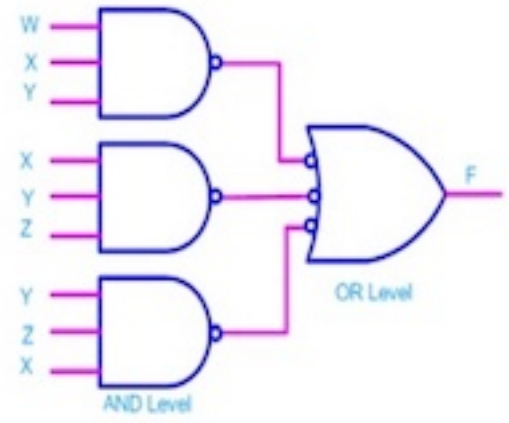
Any logic function can be implemented using NAND and NOR gates.
To achieve this, first the logic function has to be written in Sum of Product (SOP) form. Once logic function is converted to SOP, then is very easy to implement using NAND gate. In other words any logic circuit with AND gates in first level and OR gates in second level can be converted into a NAND-NAND gate circuit.

Consider the SOP expression: F = W.X.Y + X.Y.Z + Y.Z.W

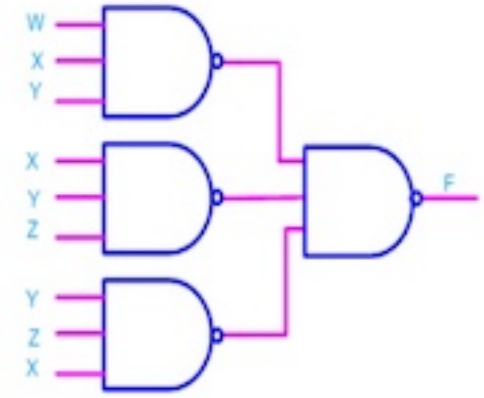
The above expression can be implemented with three AND gates in first stage and one OR gate in second stage as shown in figure.



If bubbles are introduced at AND gates output and OR gates inputs (the same for NOR gates), the above circuit becomes as shown in figure.



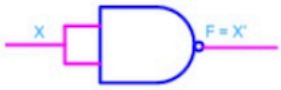
Now replace OR gate with input bubble with the NAND gate. Now we have circuit which is fully implemented with just NAND gates.



Realisation Of Logic Gates using NAND gates

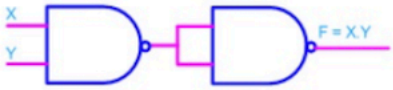
Implementing an inverter using NAND gate

Input	Output	Rule
(X.X)'	= X'	Idempotent



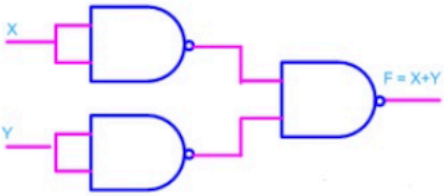
Implementing AND using NAND gates

Input	Output	Rule
((XY)'(XY)')'	= ((XY)')'	Idempotent
	= (XY)	Involution



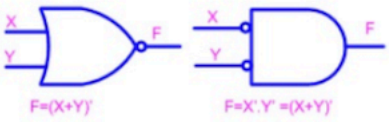
Implementing OR using NAND gates

Input	Output	Rule
((XX)'(YY)')'	= (X'Y')'	Idempotent
	= X"+Y"	DeMorgan
	= X+Y	Involution



Implementing NOR using NAND gates

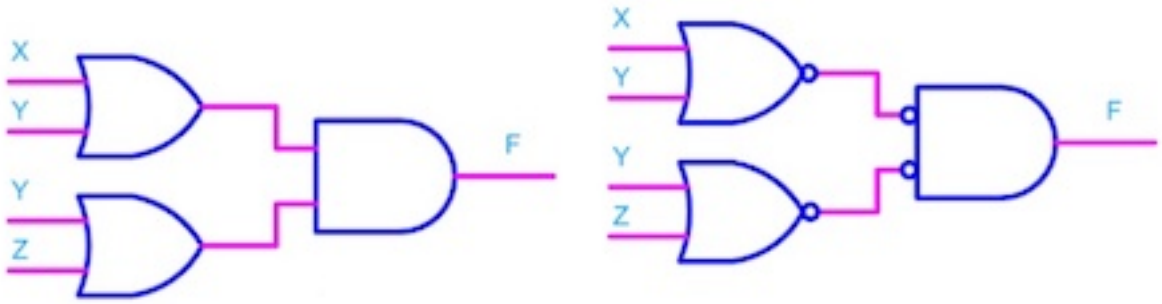
Input	Output	Rule
((XX)'(YY)')'	=(X'Y')'	Idempotent
	=X"+Y"	DeMorgan
	=X+Y	Involution
	=(X+Y)'	Idempotent



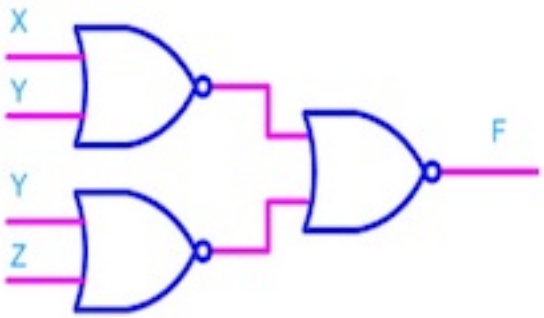
Realization of logic function using NOR gates

To achieve this, first the logic function has to be written in Product of Sum (POS) form. Once it is converted to POS, then it's very easy to implement using NOR gate. In other words any logic circuit with OR gates in first level and AND gates in second level can be converted into a NOR-NOR gate circuit.

Consider the POS expression: F = (X+Y) . (Y+Z)
The above expression can be implemented with three OR gates in first stage and one AND gate in second stage as shown in figure.



If bubble are introduced at the output of the OR gates and the inputs of AND gate, the above circuit becomes as shown in figure.
Now replace AND gate with input bubble with the NOR gate. Now we have circuit which is fully implemented with just NOR gates.

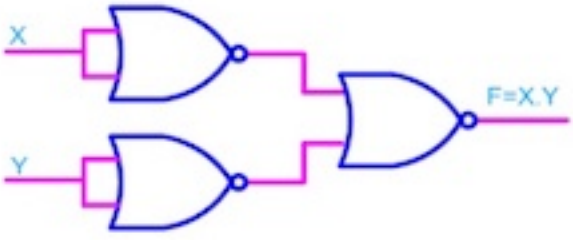


Implementing an inverter using NOR gate

Input	Output	Rule
(X+X)'	= X'	Idempotent

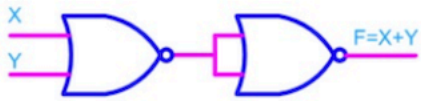
Implementing AND using NOR gates

Input	Output	Rule
((X+X)'+(Y+Y)')'	=(X'+Y')'	Idempotent
	= X".Y"	DeMorgan
	= (X.Y)	Involution



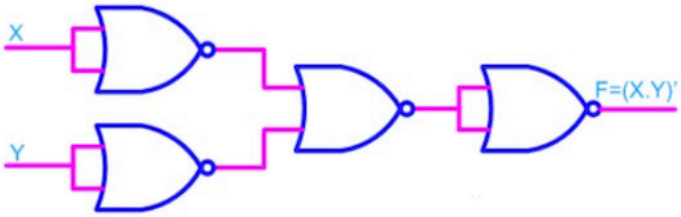
Implementing OR using NOR gates

Input	Output	Rule
((X+Y)'+(X+Y)')'	= ((X+Y)')'	Idempotent
	= X+Y	Involution



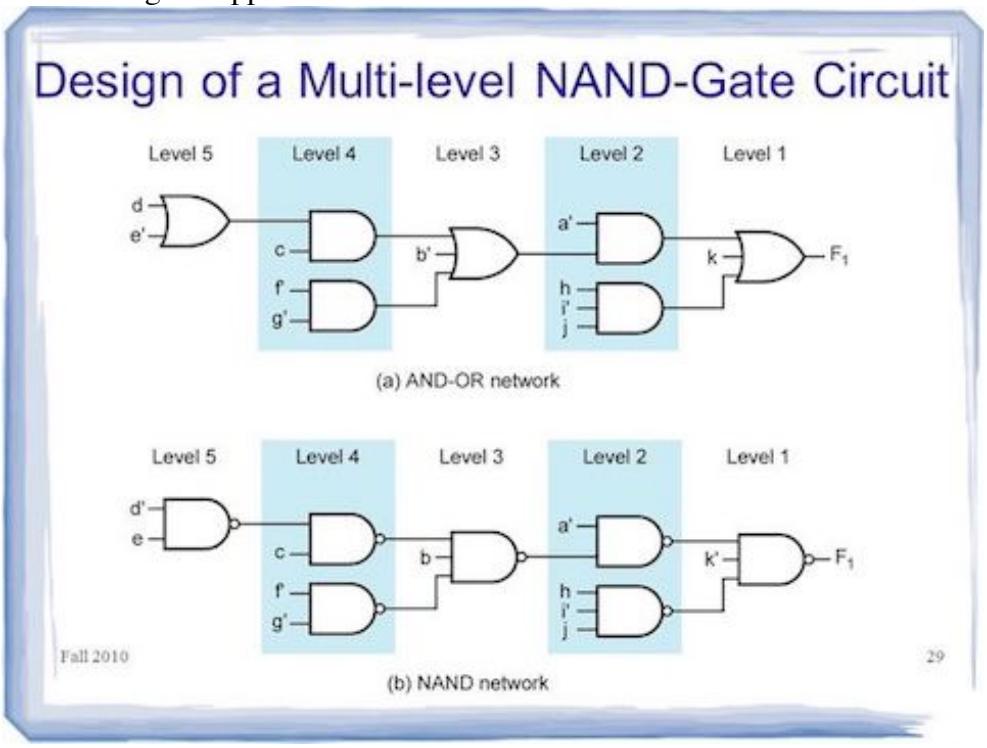
Implementing NAND using NOR gates

Input	Output	Rule
((X+Y)'+(X+Y)')'	= ((X+Y)')'	Idempotent
	= X+Y	Involution
	= (X+Y)'	Idempotent



Multilevel NAND Circuits

- Convert all AND gates to NAND gates with AND-NOT graphic symbols.
-Convert all OR gates to NAND gates with NOT-OR graphic symbols.
-Check all the bubbles in the diagram. For every bubble that is not counteracted by another bubble along the same line, insert a NOT gate or complement the input literal from its original appearance



Multilevel NOR Circuits

Starting from a multilevel circuit:

-Convert all OR gates to NOR gates with OR- NOT graphic symbols.

-Convert all OR gates to NOR gates with NOT- AND graphic symbols.

-Check all the bubbles in the diagram. For every bubble that is not counteracted by another bubble along the same line, insert a NOT gate or complement the input literal from its original appearance.