DESIGN OF SEQUENTIAL LOGIC CIRCUITS

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SEQUENTIAL LOGIC CIRCUITS

Design of SR latch Circuit

Design of clock latch and F/F Circuits

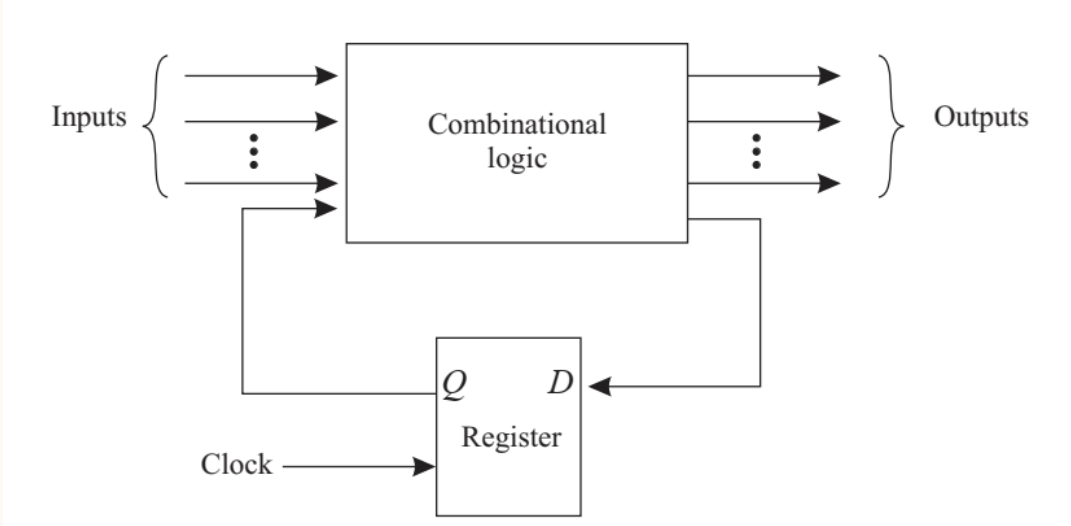
Design of clocked JK Latch

Design of CMOS D F/F

SEQUENTIAL LOGIC CIRCUITS

In the combinational logic circuits, the output is determined by the input logic levels. The combinational circuit lacks the storing capability of any previous events. In the sequential logic circuits, the output is determined by the present input logic level, as well as the past output logic level. In the sequential circuit, there is a feedback connection between the output and the input.

The generalized structure of a sequential circuit is shown in Fig. It consists of a combinational logic block and a memory circuit in the feedback path.



SEQUENTIAL LOGIC CIRCUITS

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The generalized structure of a sequential circuit is shown in Fig. It consists of a combinational logic block and a memory circuit in the feedback path.

The feedback path contains the register that has the bit storing capability. The sequential logic circuit is also known as *regenerative* logic circuit. The regenerative circuits are formed with positive feedback. They are classified into three following types:

Bistable circuits—have two stable states.

Monostable circuits—have only one stable state.

Astable circuits—have no stable state, rather they oscillate between two states.

Bistable circuits are the most commonly used circuits. Latches, flip-flops, registers, and memory are the examples of bistable circuits.

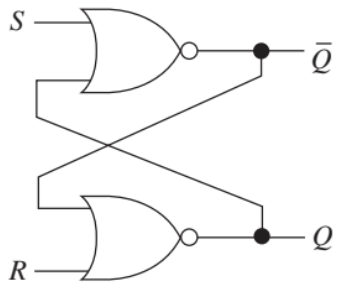
DESIGN OF SR LATCH

In the SR latch logic circuit, there are two inputs: S (Set) and R (Reset) and two complementary outputs: Q and $\overline{Q}$. The input and output relationship is described in Table

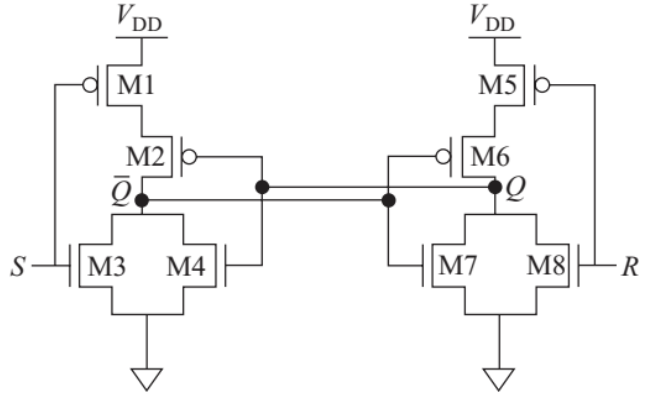
Truth table of the NOR-based SR latch circuit

S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
0	0	Q_n	$\overline{Q_n}$	Hold
1	0	1	0	Set
0	1	0	1	Reset
1	1	0	0	Not allowed

The gate-level schematic of the SR latch circuit is shown in Fig.
Figure shows the CMOS realization of the NOR-based SR latch circuit.



Gate-level schematic of SR latch realized using NOR gate



CMOS realizations of NOR-based SR latch circuit

DESIGN OF SR LATCH

The next state of SR latch can be expressed as

$Q_{n+1} = S + \bar{R}Q_n$ (for $SR = 0$)

The condition $SR = 0$ implies that both S and R cannot be 1 at the same time. An equation that expresses the next state value of a latch in terms of its present state and inputs is referred to as a 'next-state equation' or a 'characteristic equation'.

Operation When $S = 0$ and $R = 0$, the nMOS transistors M3 and M8 are OFF. The pMOS transistors M1 and M5 are ON. This cannot determine the output logic. Let us assume $Q = 0$, then M2 is ON and M4 is OFF. Thus, the node Q is connected to VDD, i.e., $Q = 1$. As $Q = 1$, M7 is ON and M6 is OFF. Thus, node Q is connected to the ground, i.e., Q remains at logic 0 state. If we assume $Q = 1$, then M4 is ON and M2 is OFF. Thus, node Q is connected to the ground, i.e., $Q = 0$. As $Q = 0$, M6 is ON and M7 is OFF. Thus, node Q is connected to VDD, i.e., Q remains at logic 1 state. This proves the first row of the truth table of SR latch.

DESIGN OF SR LATCH

When $S = 0$, $R = 1$, the transistor M8 is ON. Thus, irrespective of other input and past output conditions, the node Q is connected to the ground, i.e., Q is in logic 0 state.

When $S = 1$ and $R = 0$, the transistor M3 is ON. Thus, irrespective of other input and past output conditions, the node Q is connected to the ground, i.e., Q is in logic 0 state. This makes M5 and M6 ON; thus, node Q is connected to VDD, i.e., Q is in logic 1 state.

DESIGN OF SR LATCH

If S and R inputs are zero at the same time, both the outputs will be zero. Hence, this combination is not allowed.

The SR latch circuit can also be realized using NAND gates as shown in Fig. 6.30.

Table 6.5 shows the truth table of NAND-based SR latch circuit.

Figure 6.31 shows the CMOS realization of the NAND-based SR latch circuit.

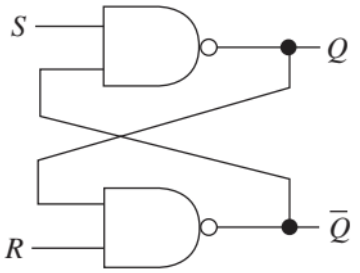


Fig. 6.30 Gate-level schematic of SR latch realized using NAND gate

Table 6.5 Truth table of the NAND-based SR latch circuit

S	R	Q_{n+1}	$\overline{Q}_{n+1}$	Operation
0	0	1	1	Not allowed
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q_n	$\overline{Q}_n$	Hold

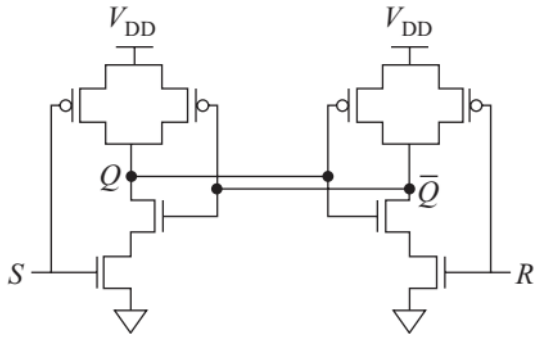
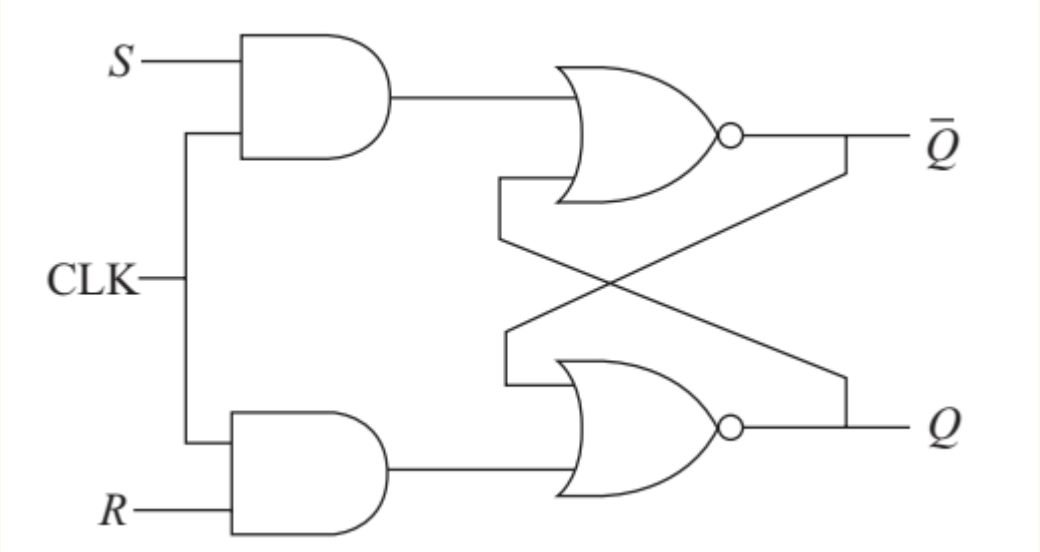


Fig. 6.31 CMOS realizations of NAND-based SR latch circuit

DESIGN OF CLOCKED LATCH AND F/F CKT

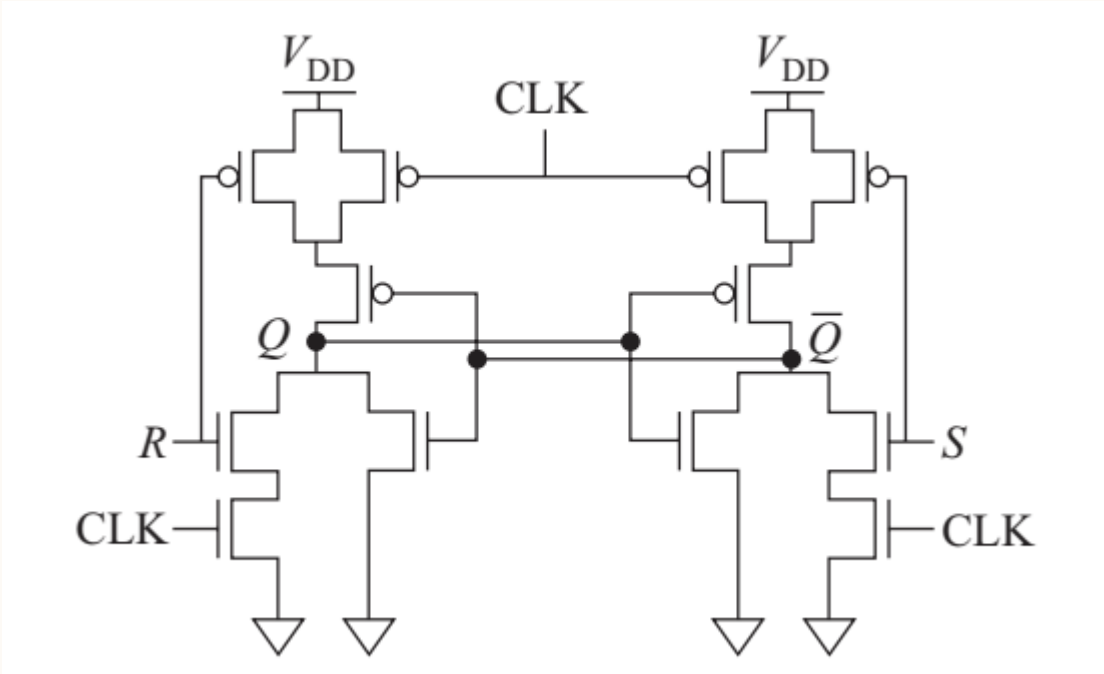
The SR latch circuits discussed in Section 6.10.1 are asynchronous in nature in which the output changes as the input logic level changes. In a design, the inputs might come from different paths encountering different path delays. Hence, depending on which input comes first, the output might change accordingly, which might not be the desirable output. To avoid this problem, a clock input is added such that the output changes only in the active period of the clock signal. Generally, the clock signal is a periodic square waveform applied simultaneously to all the gates in the system.

Figure shows the gate-level schematic of the clocked NOR-based SR latch.



DESIGN OF CLOCKED LATCH AND F/F CKT

Figure below shows the CMOS design of the NOR-based SR latch circuit.



DESIGN OF CLOCKED JK F/F CKT

The JK latch is commonly known as JK flip-flop. It has three inputs: J, K, and CLK; and two complementary outputs: *Q* and *Q*. JK flip-flop has no not-allowed inputs, unlike SR latches. It allows all possible input combinations. The truth table is shown in Table

Truth table of JK flip-flop

J	K	Q_n	$\overline{Q}_n$	Q_{n+1}	$\overline{Q}_{n+1}$	Operation
0	0	0	1	0	1	Hold
		1	0	1	0	
0	1	0	1	0	1	Reset
		1	0	0	0	
1	0	0	1	1	0	Set
		1	0	1	0	
1	1	0	1	1	0	Toggle
		1	0	0	1	

DESIGN OF CLOCKED LATCH AND F/F CKT

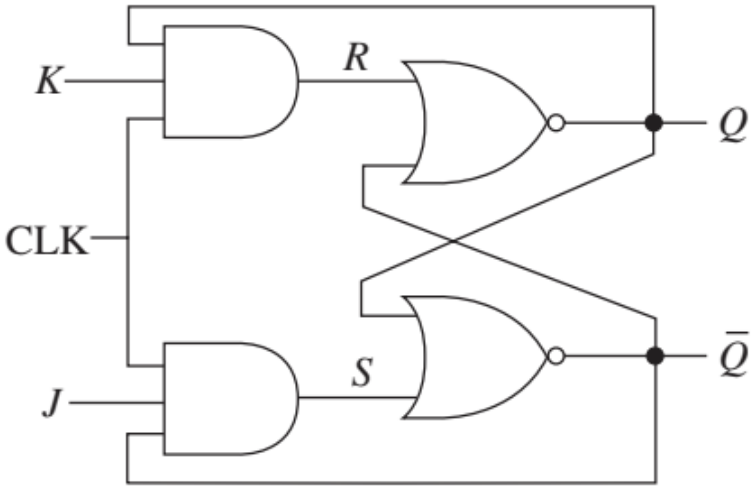
Figure below shows the gate-level design of the JK flip-flop.

From the gate-level design of JK flip-flop shown in Fig. 6.34, we can write the expressions for the output as

$$\bar{Q} = \overline{S + Q} = \overline{\bar{Q} \cdot J \cdot CLK + Q}$$

$$Q = \overline{R + \bar{Q}} = \overline{Q \cdot K \cdot CLK + \bar{Q}}$$

Therefore, to implement the PDN for implementing the logic for Q, we require three nMOS transistors connected in series with one nMOS connected in parallel. The inputs to the series connected nMOS transistors are Q, K, and CLK and the input to the parallel connected nMOS transistor is Q.



DESIGN OF CLOCKED LATCH AND F/F CKT

Similarly, to implement the PDN for implementing the logic for *Q*, we require three nMOS transistors connected in series with one nMOS connected in parallel. The inputs to the series connected nMOS transistors are *Q*, *J*, and CLK and the input to the parallel connected nMOS transistor is *Q*.

Figure below shows the CMOS design of the JK flip-flop.