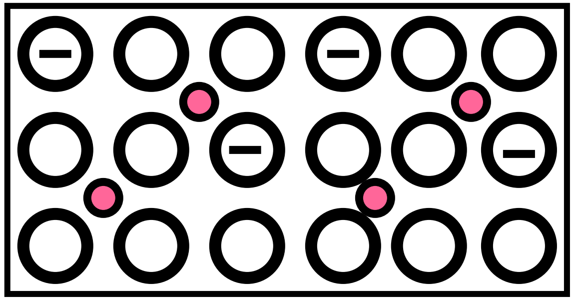
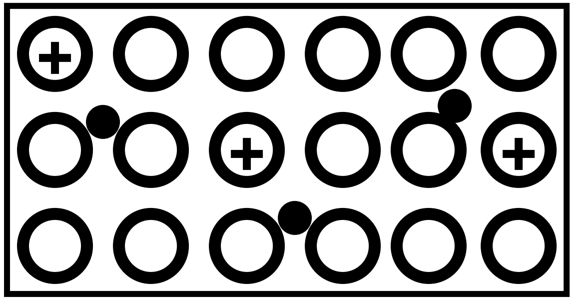
# p-n junctions

# p-n junction formation





**p-type material**

Semiconductor material doped with **acceptors**.

Material has high hole concentration

Concentration of free electrons in p-type material is very low.

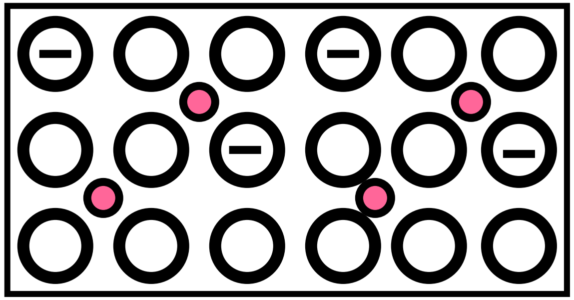
**n-type material**

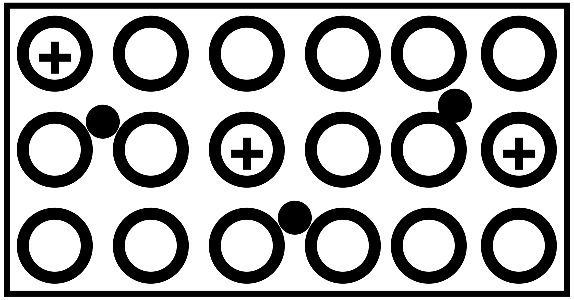
Semiconductor material doped with **donors**.

Material has high concentration of free electrons.

Concentration of holes in n-type material is very low.

# p-n junction formation





**p-type material**

Contains NEGATIVELY charged acceptors (immovable) and POSITIVELY charged holes (free).

Total charge = 0

**n-type material**

Contains POSITIVELY charged donors (immovable) and NEGATIVELY charged free electrons.

Total charge = 0

# p-n junction formation

What happens if n- and p-type materials are in close contact?

**p-type material**

Contains NEGATIVELY charged acceptors (immovable) and POSITIVELY charged holes (free).

Total charge = 0

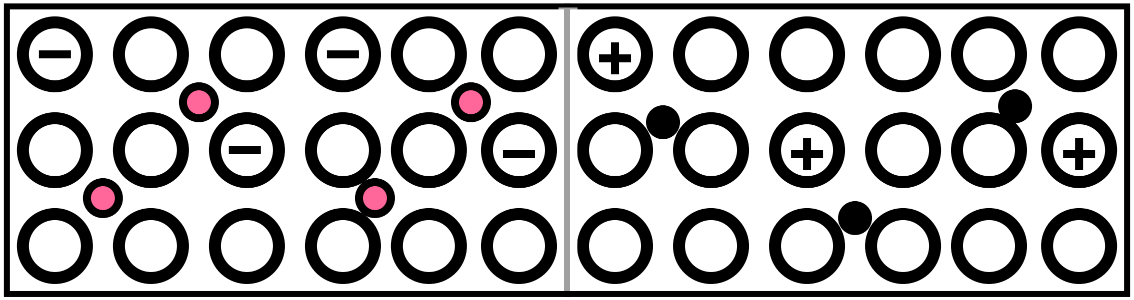
**n-type material**

Contains POSITIVELY charged donors (immovable) and NEGATIVELY charged free electrons.

Total charge = 0

# p- n junction formation

**What happens if n- and p-type materials are in close contact?**



Being free particles, **electrons** start diffusing from n-type material into p-material

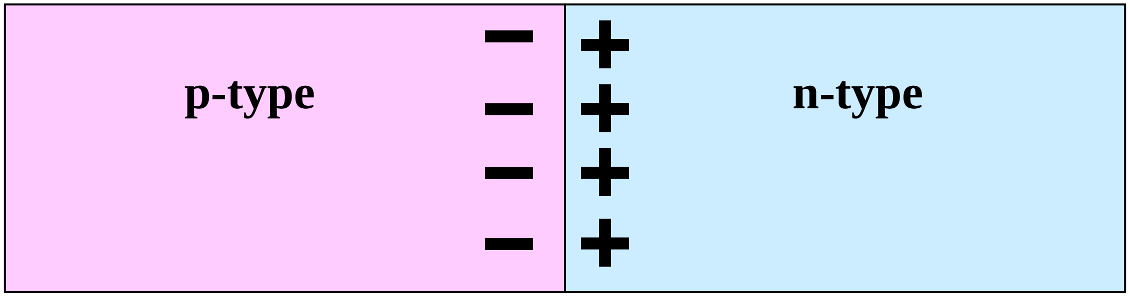
Being free particles, **holes,** too**,** start diffusing from p-type material into n-material

Have they been NEUTRAL particles, eventually all the free electrons and holes had uniformly distributed over the entire compound crystal.

However, every electrons transfers a negative charge (-q) onto the p-side and also leaves an uncompensated (+q) charge of the donor on the n-side.
Every hole creates one positive charge (q) on the n-side and (-q) on the p-side

# p- n junction formation

**What happens if n- and p-type materials are in close contact?**



Electrons and holes remain staying close to the p-n junction because negative and positive charges attract each other.

Negative charge stops electrons from further diffusion

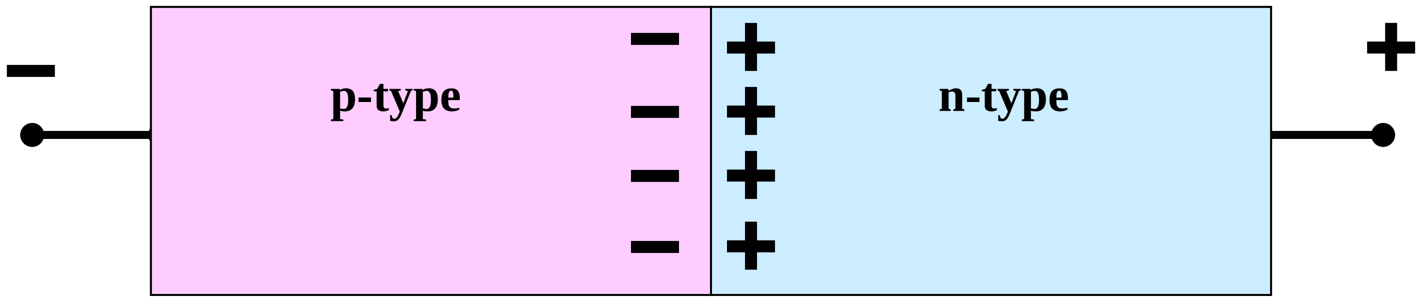
Positive charge stops holes from further diffusion

**The diffusion forms a dipole charge layer at the p-n junction interface.**

**There is a "built-in" VOLTAGE at the p-n junction interface that prevents penetration of electrons into the p-side and holes into the n-side.**

# p- n junction current – voltage characteristics

**What happens when the voltage is applied to a p-n junction?**



The polarity shown, attracts holes to the left and electrons to the right.

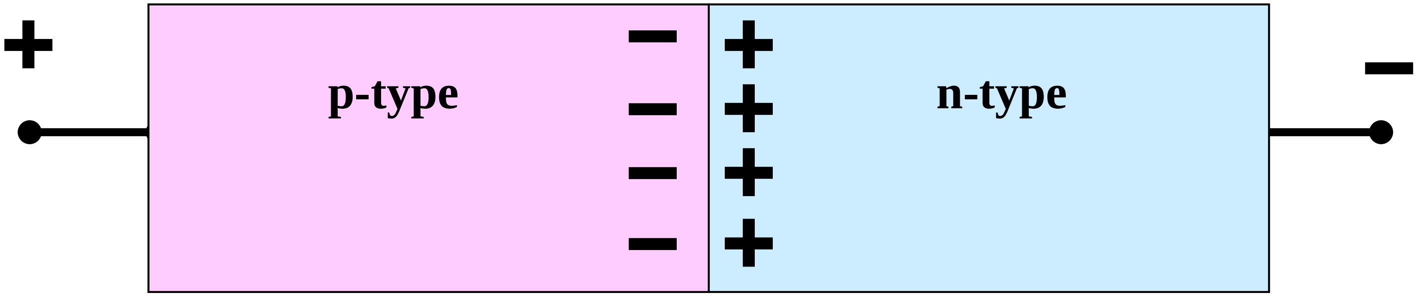
According to the **current continuity law,** the current can **only** flow if all the charged particles move forming a closed loop

However, there are very few holes in n-type material and there are very few electrons in the p-type material.
There are very few carriers available to support the current through the junction plane

**For the voltage polarity shown, the current is nearly zero**

# p- n junction current – voltage characteristics

**What happens if voltage of opposite polarity is applied to a p-n junction?**



The polarity shown, attracts electrons to the left and holes to the right.

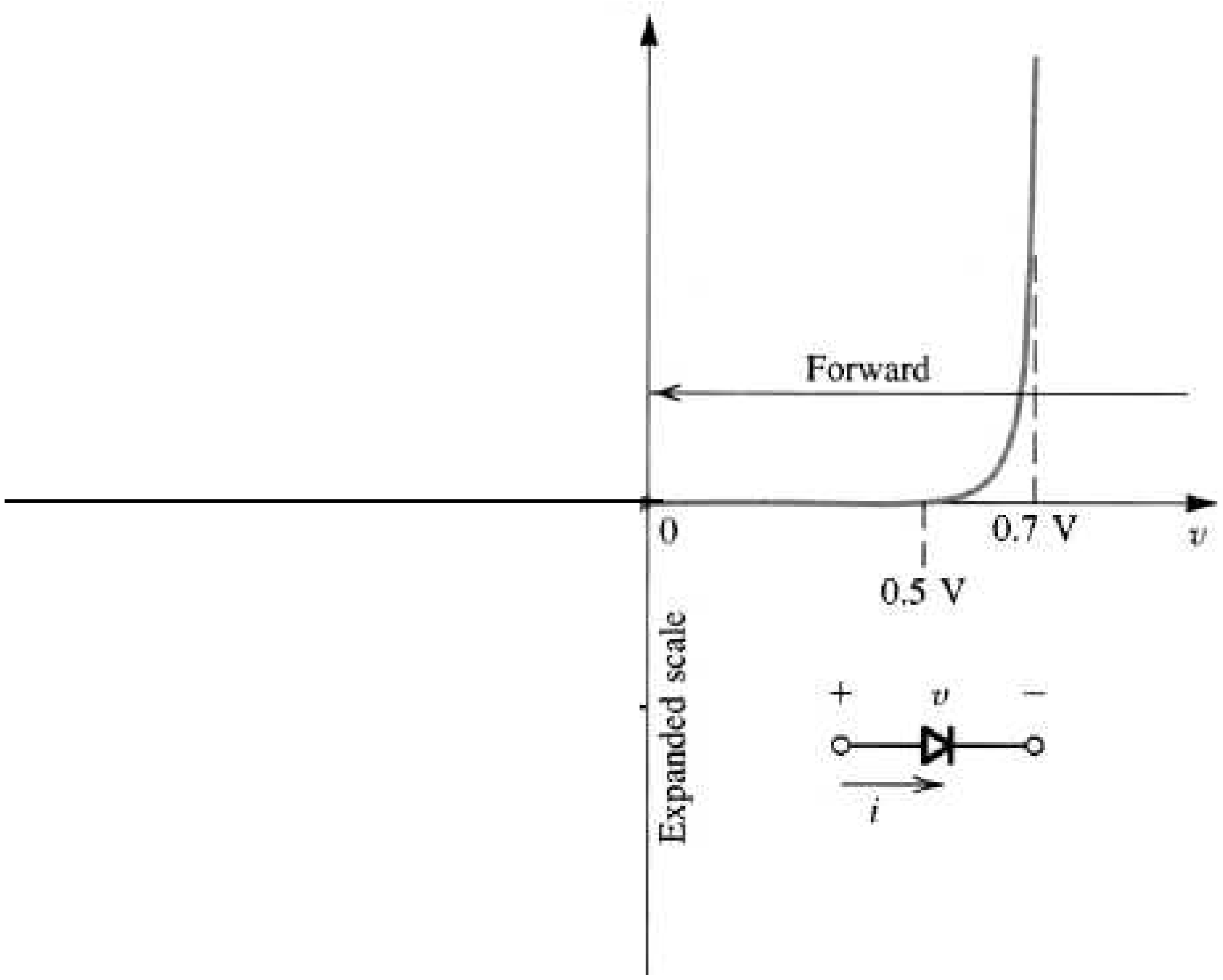
There are plenty of electrons in the n-type material and plenty of holes in the p-type material.

There are a lot of carriers available to cross the junction.

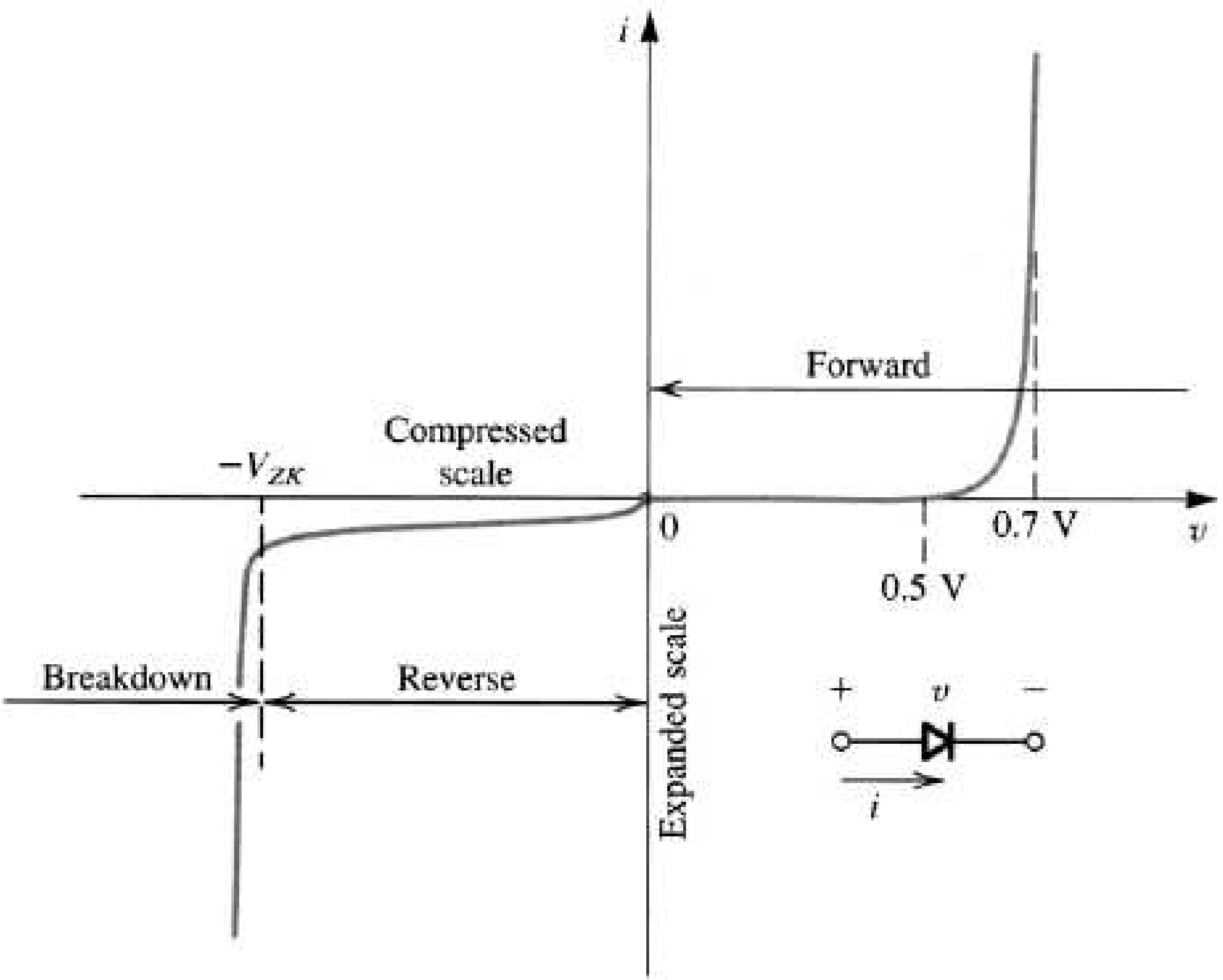
**When the applied voltage is lower than the built-in voltage, the current is still nearly zero**

**When the voltage exceeds the built-in voltage, the current can flow through the p-n junction**

# The experimental I-V characteristic of a Si diode



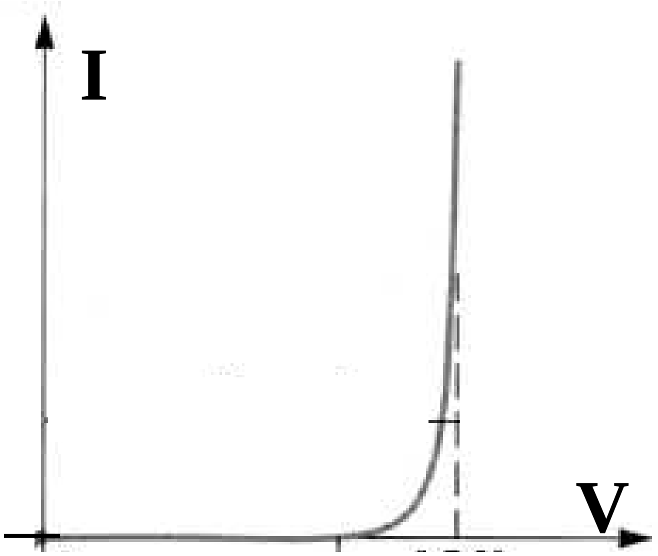
# The experimental I-V characteristic of a Si diode



The diode *i*–*v* relationship with some scales expanded and others compressed in order to reveal details.

# I-V characteristic of an ideal p-n junction diode

$$I = I_S\left[\mathbf{exp}\left(\frac{qV}{kT}\right) - 1\right]$$



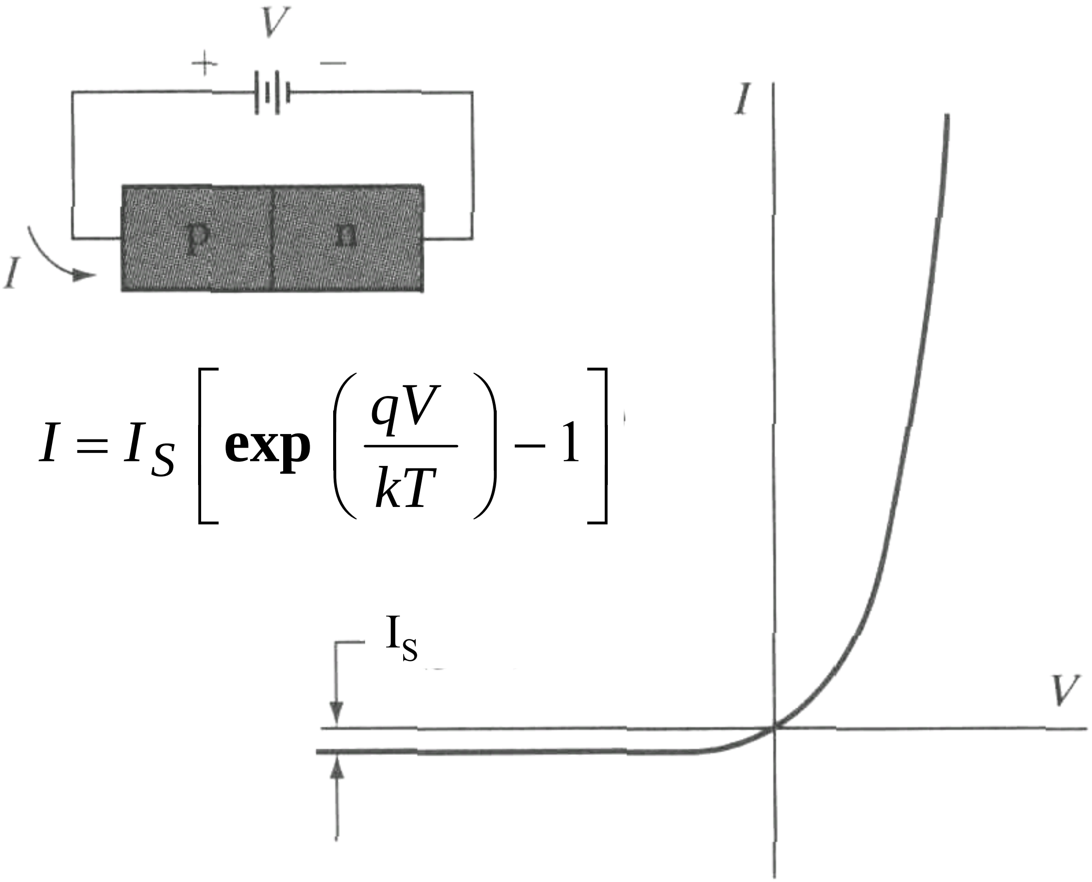
k is the Boltzmann constant
T is the temperature in K.
At room temperature (T ≈ 300 K),
***(kT/q) ≈ 0.026 V***

$I_S$ is a ***saturation current***. Typically, $I_S$ is very small: $I_S \approx 10^{-17} \ldots 10^{-11}$ A

When the voltage V is negative ("reverse" polarity) the exponential term ≈ -1;
The diode current is ≈ $I_S$ ( very small).

When the voltage V is positive ("forward" polarity) the exponential term increases rapidly with V and the current is high.

# The I-V characteristic of the diode

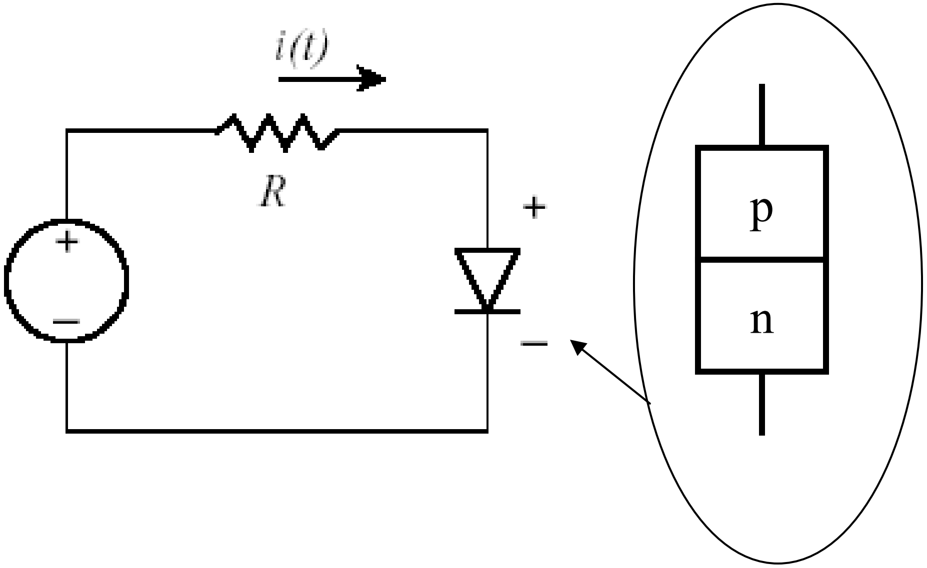


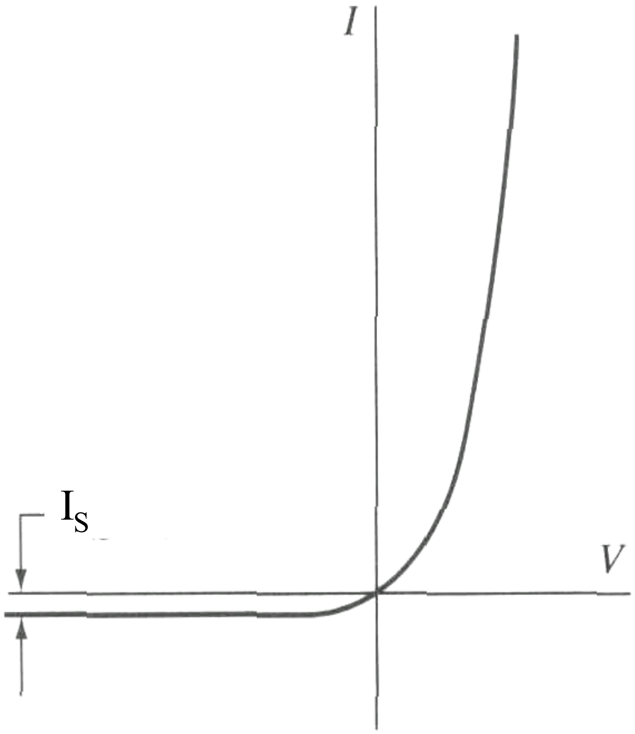
$$I = I_S\left[\mathbf{exp}\left(\frac{qV}{kT}\right) - 1\right]$$

At room temperature, the I-V expression reduces to:

$$I = I_S\left[\mathbf{exp}\left(\frac{V}{0.026}\right) - 1\right]$$

# p- n diode circuit notation

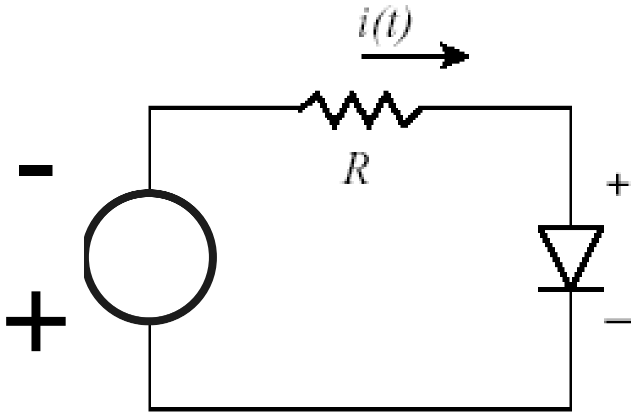


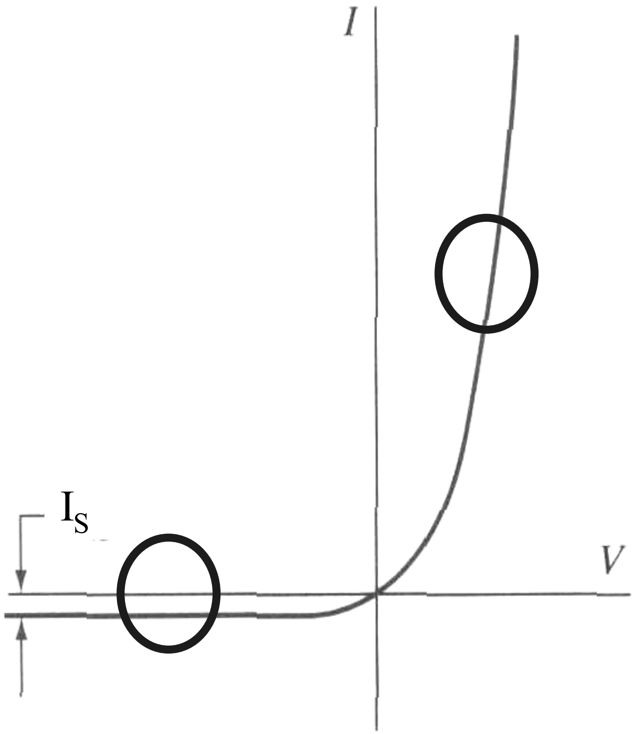


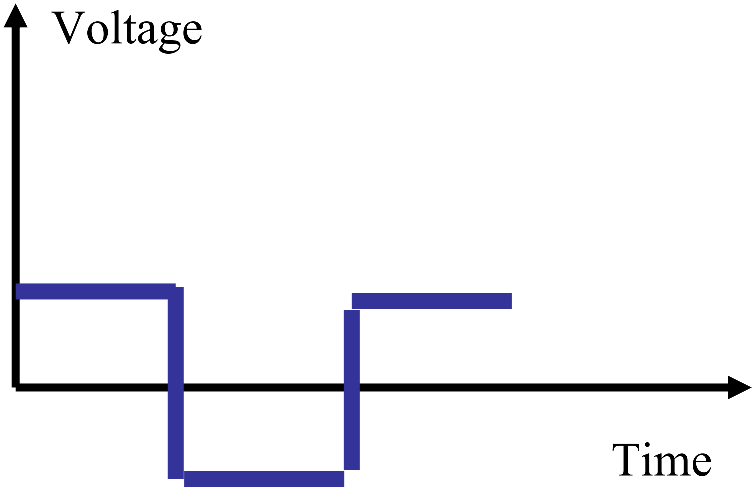
**When "plus" is applied to the p-side, the current is high. This voltage polarity is called FORWARD.**

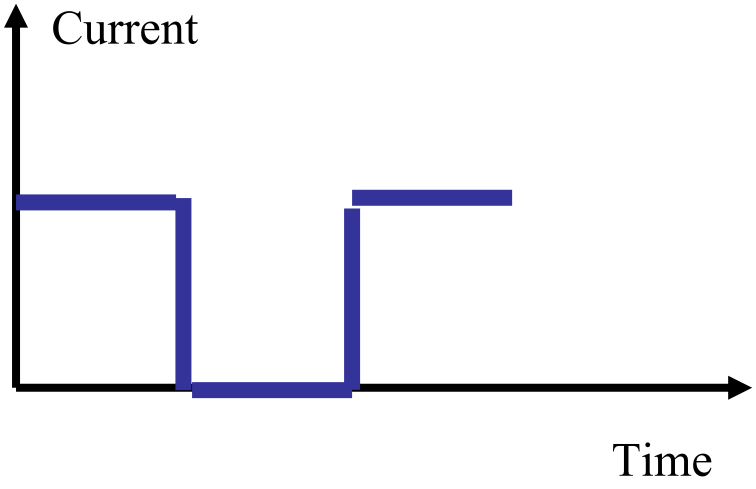
**When "plus" is applied to the n-side, the current is nearly zero. This voltage polarity is called REVERSE.**

# p- n diode applications: current rectifiers

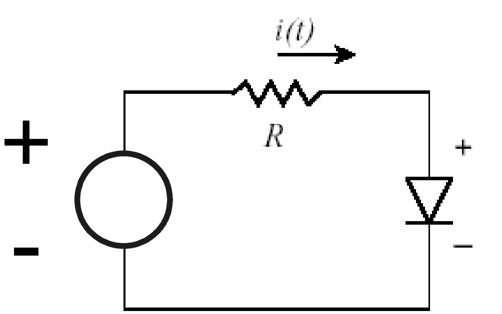




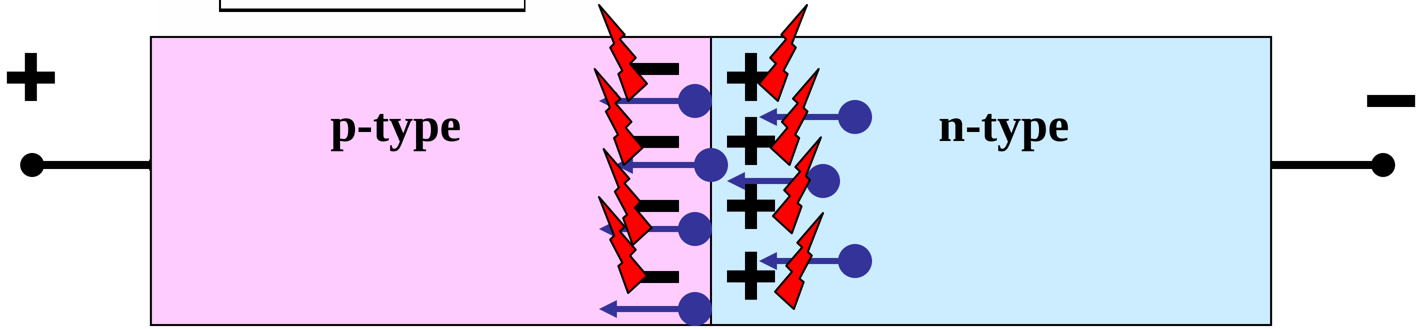




# p- n diode applications: Light emitters



**P-n junction can emit the light when forward biased**



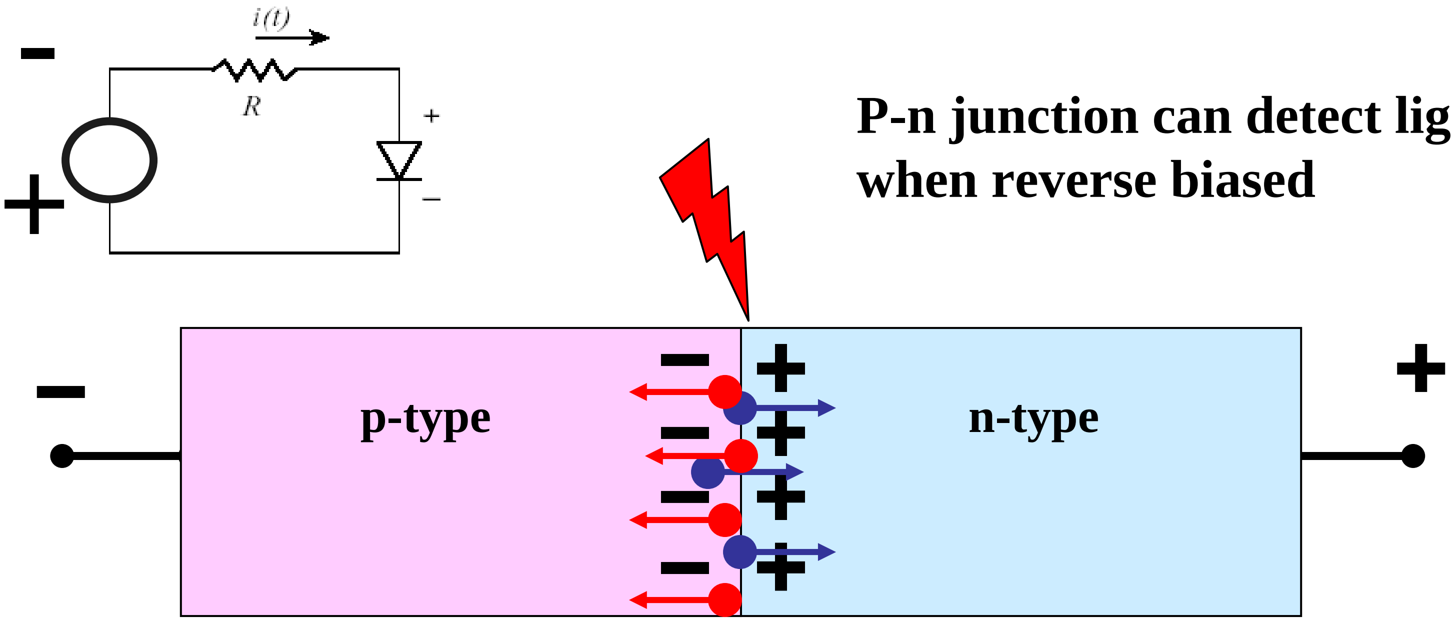
Electrons drift into p-material and find plenty of holes there. They “RECOMBINE” by filling up the “empty” positions.

Holes drift into n-material and find plenty of electrons there. They also “RECOMBINE” by filling up the “empty” positions.

The energy released in the process of “annihilation” produces

PHOTONS – the particles of light

# p- n diode applications: Photodetectors



**P-n junction can detect light when reverse biased**

When the light illuminates the p-n junction, the photons energy RELEASES free electrons and holes.

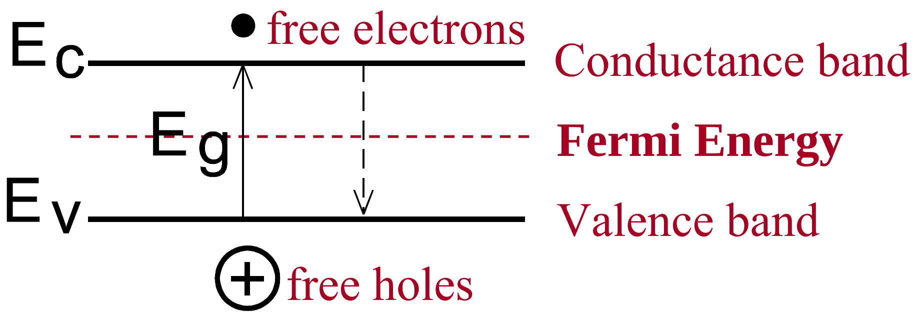
They are referred to as PHOTO-ELECTRONS and PHOTO-HOLES

The applied voltage separates the photo-carriers attracting electrons toward “plus” and holes toward “minus”

As long as the light is ON, there is a current flowing through the p-n junction

# Band diagrams and built-in voltage of the p-n junction

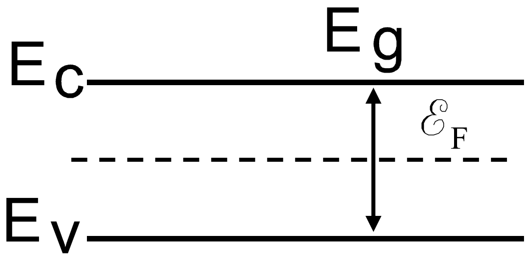
# Semiconductor Energy Bands and Fermi Energy concept

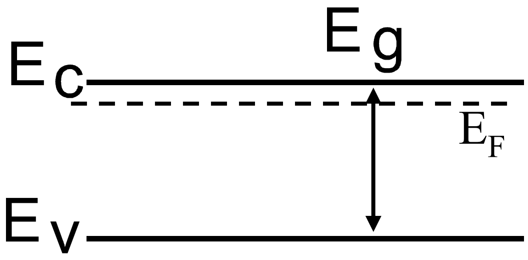


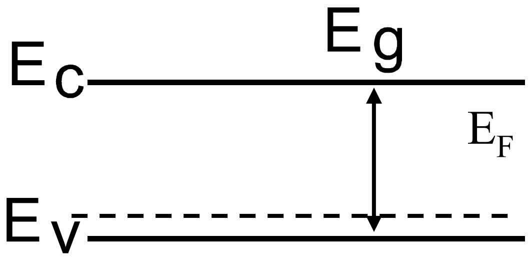
**Fermi Energy $E_F$ is an average energy of all the free carriers in a sample.**

**In equilibrium, the Fermi Energy MUST be uniform over the semiconductor sample**
**(compare to the temperature distribution over any sample in equilibrium)**

# Fermi level position in doped semiconductors







Intrinsic semiconductor:

$n = p = n_{i;}$

$\mathscr{E}_F \sim (\mathscr{E}_C + \mathscr{E}_V)/2$

Donor doped semiconductor (n-type):

$n >> p$

$\mathscr{E}_F \sim \mathscr{E}_C$

Acceptor doped semiconductor (p-type):

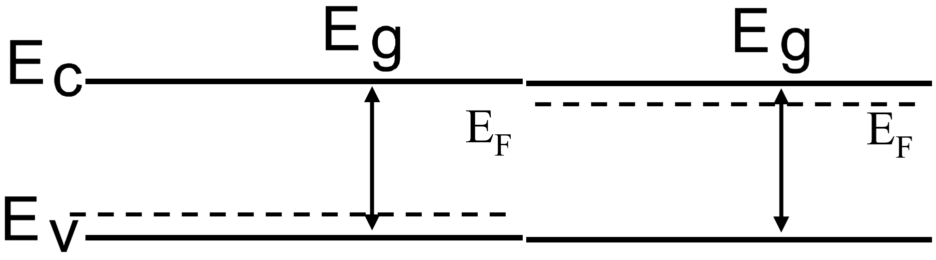
$p >> n$

$\mathscr{E}_F \sim \mathscr{E}_V$

# Formation of the p-n junction: the energy band diagram language

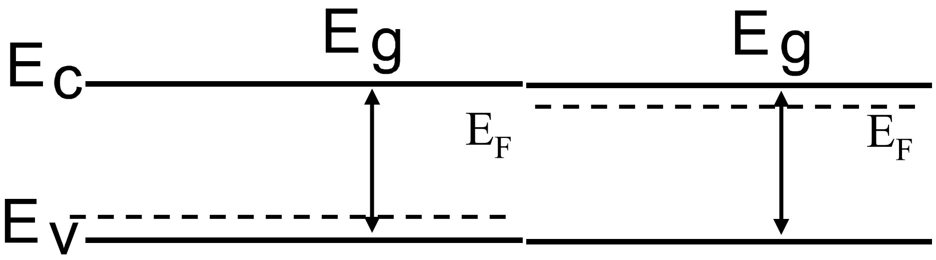
1. Two separate bits of semiconductor, one is an n-type, the other is a p-type

2. Bits joined together: not in equilibrium yet! $E_F(n) \neq E_F(p)$



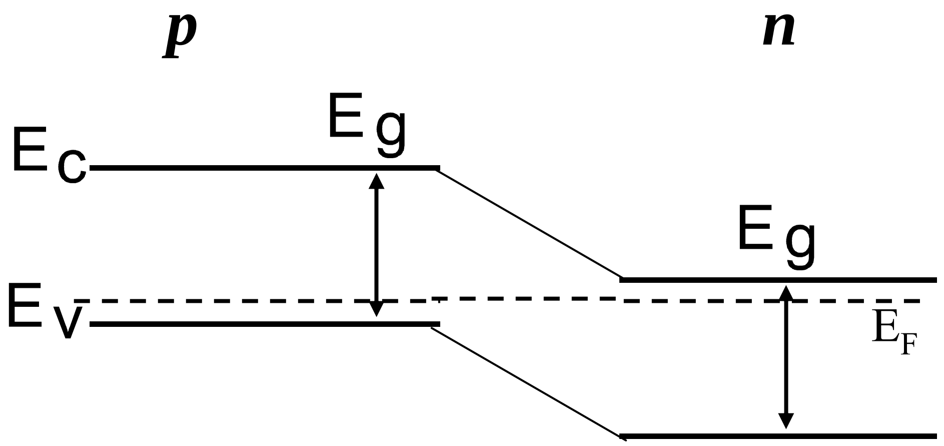
# Formation of the p-n junction: the energy band diagram language

3. Junction comes into the equilibrium by balancing the Fermi level



# Formation of the p-n junction: the energy band diagram language

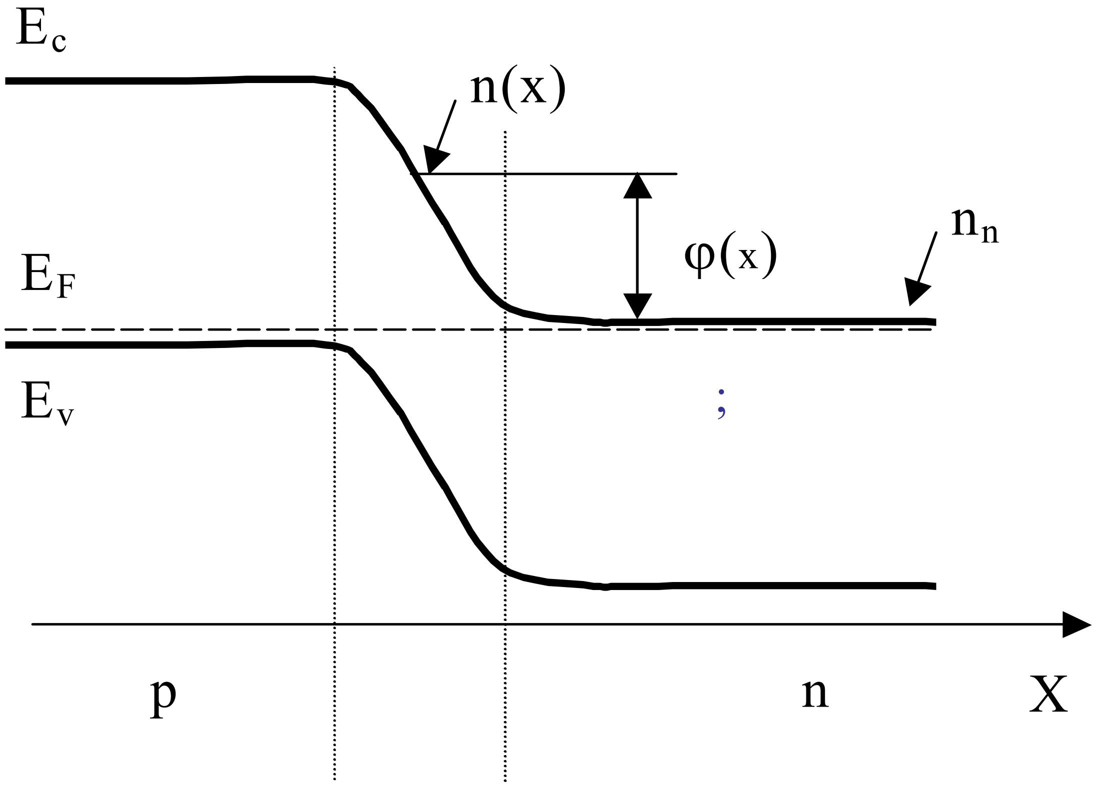
3. Junction coming to the equilibrium by balancing the Fermi level



The balance is achieved by electrons diffusing into a p-side (bringing an extra negative charge in there) and by the holes diffusing into an n-side (bringing an extra negative charge in there)

# Built-in voltage of the p-n junction

**The voltage drop between n- and p- parts, $V_{bi}$ creates a difference in the electron and hole energies, $\phi_{bi} = q \times V_{bi}$**



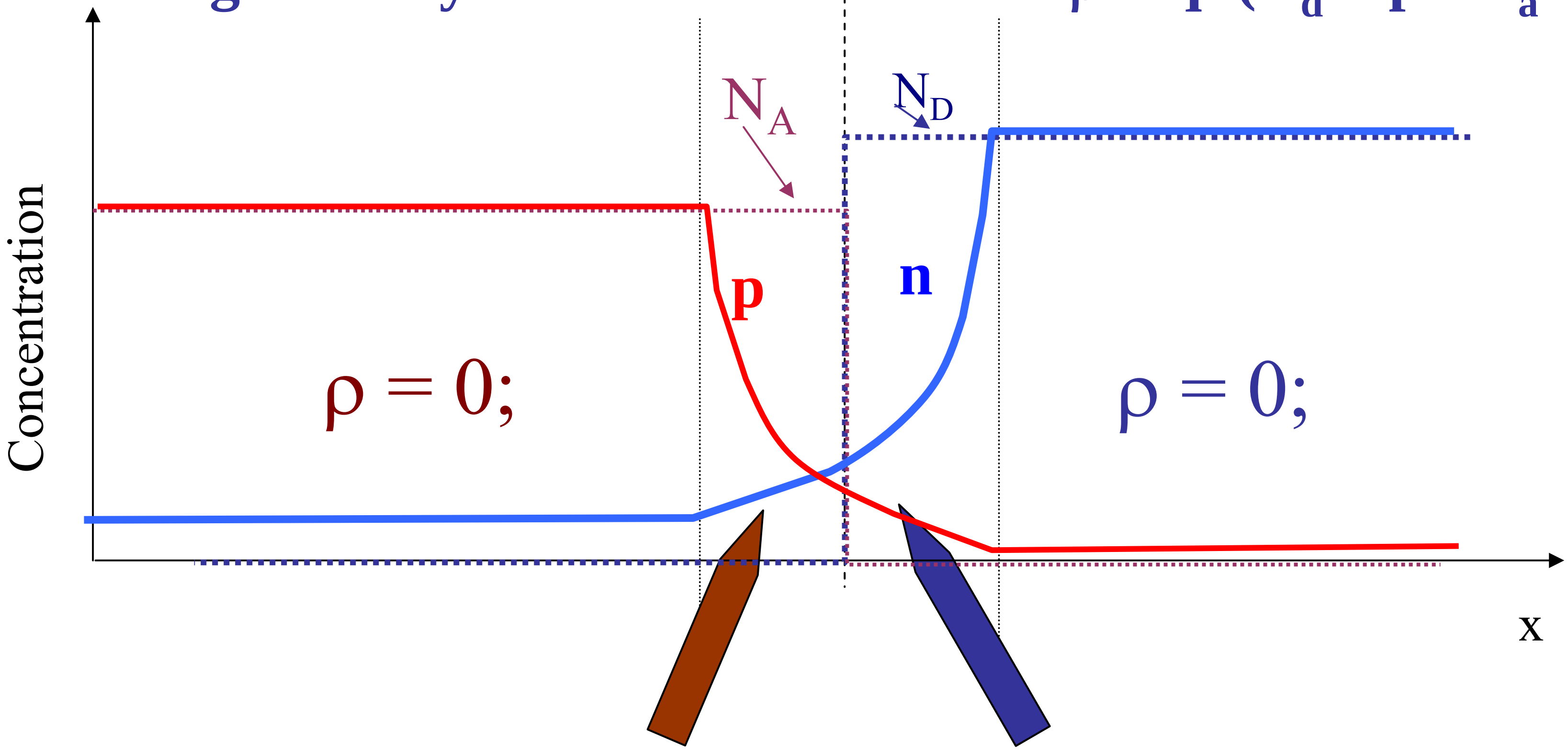
$$n \sim e^{-\frac{\varphi}{kT}}$$

$$n(x) = n_n \, e^{-\frac{\varphi(x)}{kT}}$$

$E_C$(p-side) = $E_C$(n-side) + $\varphi_{bi}$

# Charge distribution in the depletion region.

**Total charge density in the semiconductor:** $\rho = q\times(N_d + p - N_a - n)$;



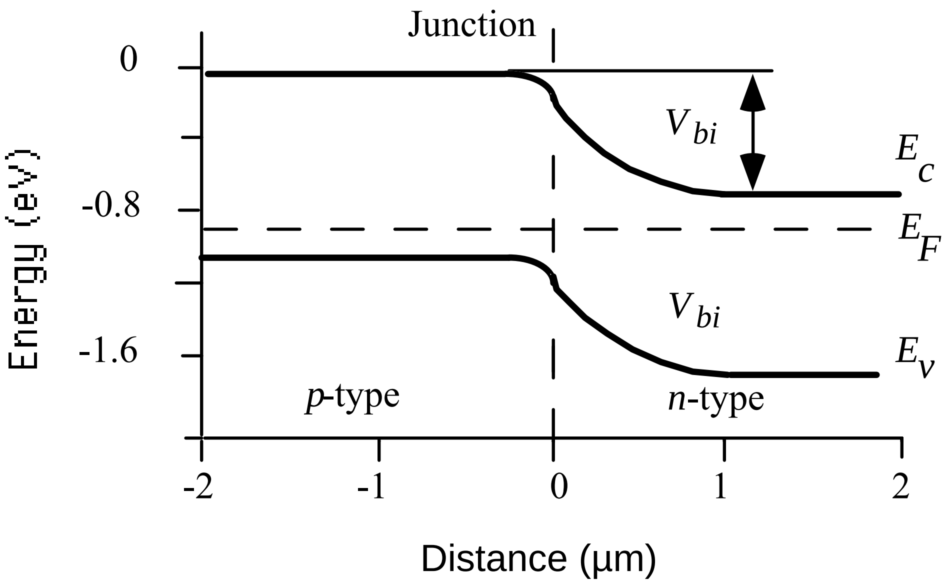
$p_n$ 0;
$n_p \approx 0$;

$\rho \approx -q\,N_A$;

$n_n \approx 0$;
$p_n \approx 0$;

$\rho \approx +q\,N_D$;

# Simulated Electron - Hole profile in Si p-n junction

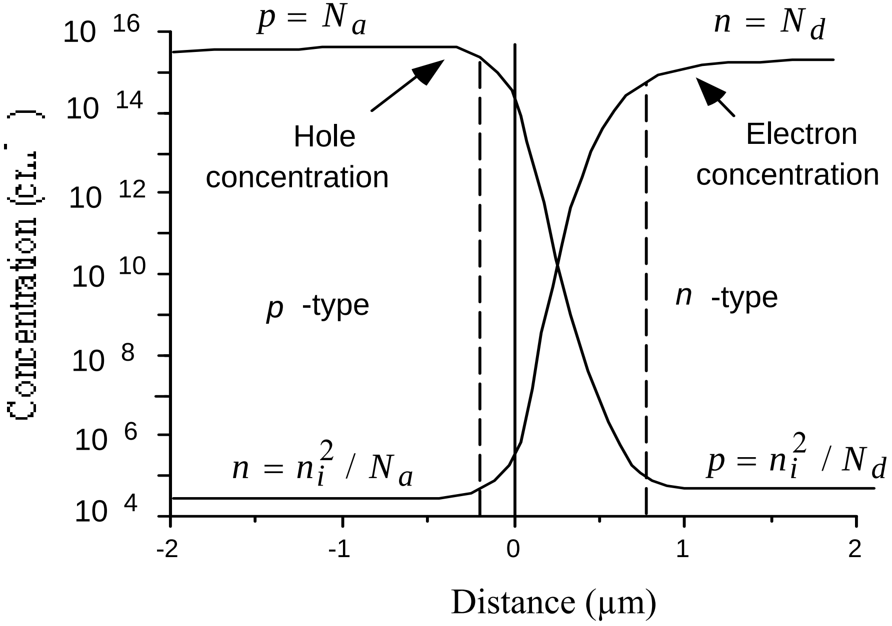


**Electron-hole concentration in a Si p-n junction.**

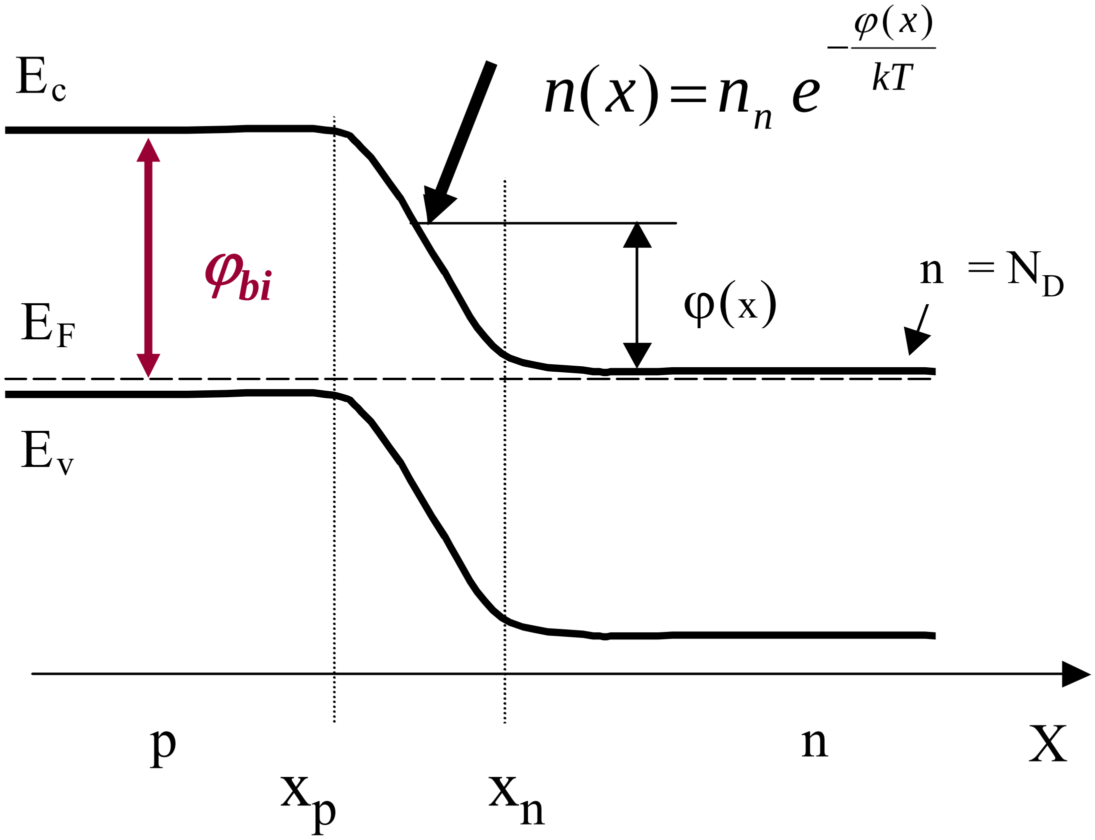
**Acceptor density $N_a=5\times10^{15}$ cm$^{-3}$**
**Donor density $N_d=1\times10^{15}$ cm$^{-3}$.**

**T=300K.**

**Dashed line show the boundaries of the depletion region**



# Built-in voltage calculation



$$n(x) = n_n\, e^{-\frac{\varphi(x)}{kT}}$$

**Far from the junction, on the n-side, n = $N_D$**

**At any arbitrary point *x* inside the transition region (between $x_n$ and $x_p$):**

$$n(x) = N_D\, e^{-\frac{\varphi(x)}{kT}}$$

**where *φ (x)* is the potential barrier at the point *x***

**At the point located far in the p-region, the potential barrier flattens out and reaches $\phi_{bi}$; at this point:**

$$n_p = N_D\, e^{-\frac{\varphi_{bi}}{kT}}$$

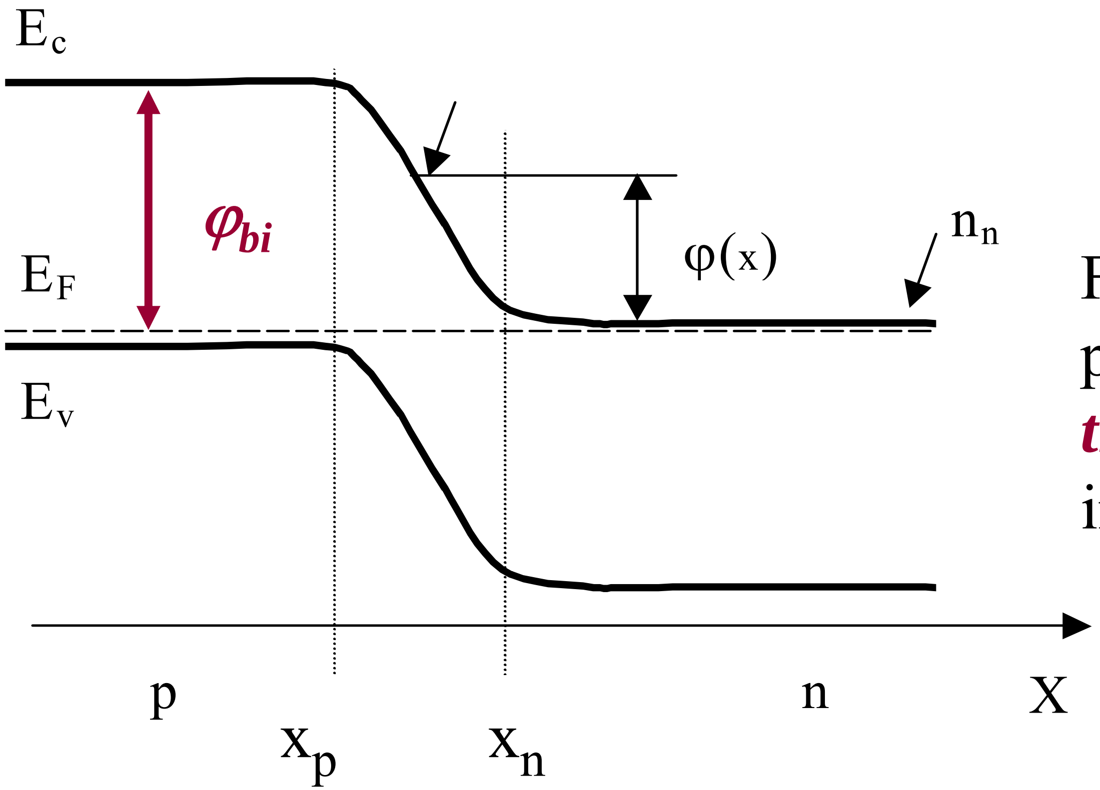
**On the other hand, for the point in the p-material:**

$$n_p = \frac{n_i^2}{N_A}$$

**Requiring both values of $n_p$ to be equal:**

$$n_p = \frac{n_i^2}{N_A} = N_D\, e^{-\frac{\varphi_{bi}}{kT}}$$

# Built-in voltage calculation



$$n_p = \frac{n_i^2}{N_A} = N_D\, e^{-\frac{\varphi_{bi}}{kT}}$$

From this, the built potential barrier, i.e. ***the energy barrier***, in Joules or eV:

$$\boxed{\varphi_{bi} = kT \cdot \ln\left(\frac{N_D N_A}{n_i^2}\right)}$$

The voltage corresponding to the energy barrier: $V_{bi} = \varphi_{bi} / q$, *or:*

$$\boxed{V_{bi} = \frac{kT}{q} \cdot \ln\left(\frac{N_D N_A}{n_i^2}\right)}$$

# Example

**Find the built-in voltage for a Si p-n junction with**

**$N_A = 10^{15}$ cm$^{-3}$ and $N_D = 10^{17}$ cm$^{-3}$**

**Assume $n_i = 10^{10}$ cm$^{-3}$;**

$$V_{bi} = \frac{kT}{q} \ln\left( \frac{N_D N_A}{n_i^2} \right)$$

Important values to remember!

At room temperature, T ≈ 300 K,

$kT \approx 0.026$ eV, $(kT/q) = 0.026$ V

Answer:
$V_{bi} = 0.718$ V