3

Junctions:-

* **Fabrication of Junctions:-** Mainly following techniques are used for fabrication of junctions-

→ 1. Grown junctions.
→ 2. alloyed junctions
→ 3. Diffused junctions
→ 4. Ion Implantation.
→ 5. Epitaxyle Junctions

⇒ **Grown junctions :-** Grown junctions are fabricated by using crystal growth process. In this process a single crystal of silicon is obtained. As we already know that silicon achieved from sand. under following steps-

Sand + Cake + Furnace heat → Refining to Improve Impurity → MGS (Metallic Grade silicon)

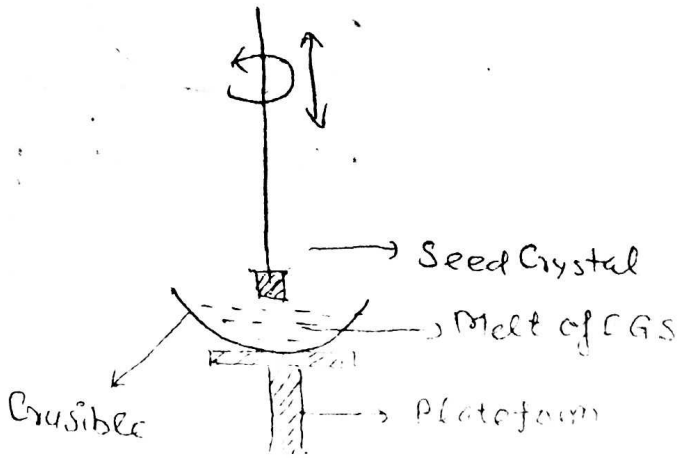
This metallic grade silicon is impure and polly crystalline.

Metallic Grade Silicon —under treatment→ Electron Grade Silicon (EGS) Pure upto [illegible] But polly crystal

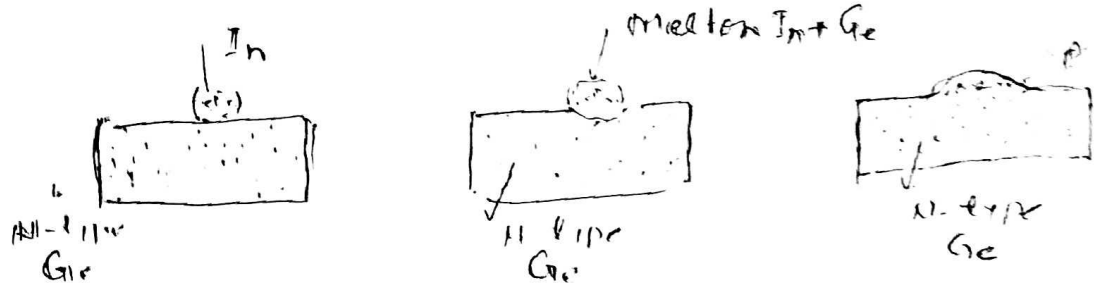
CZ process:- CZ process is used for converting this EGS into Single Crystal Silicon.

Required amount of Impurity is added for N type & P type Semiconductor.

Firstly Boron is added and growth process is stop and then further phosphorous is added.



Alloyed junctions : Alloyed junctions are fabricated by using alloying technique. In this technique a metal is alloyed on a semiconductor with the opposite type of dopant.



(a) Pellet of In in contact with N type Ge.

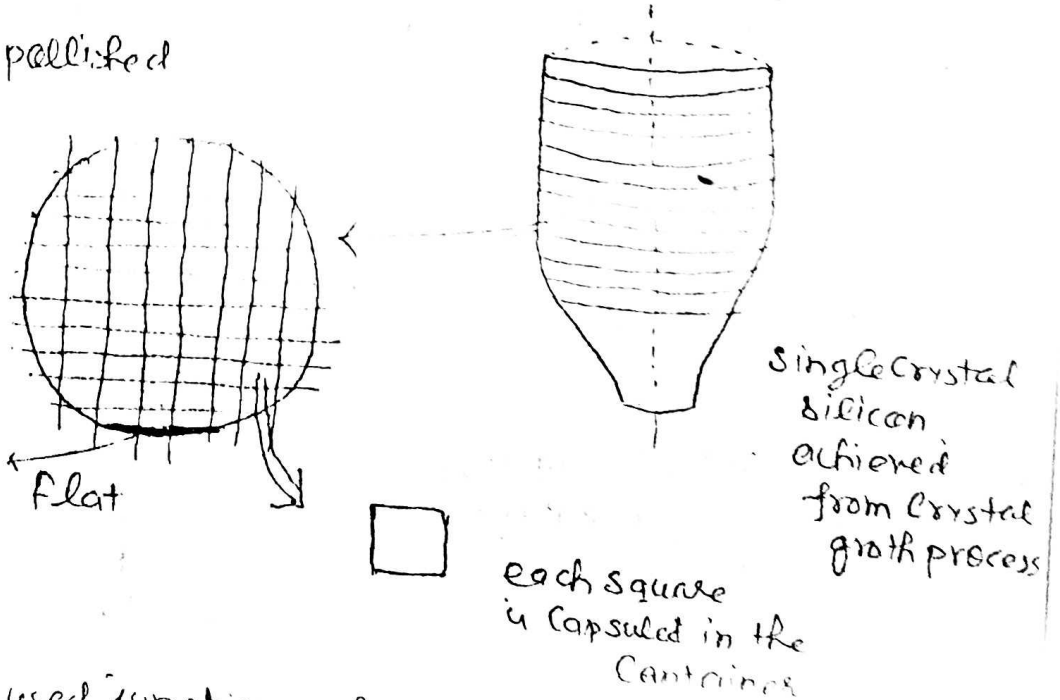
(b) Molten phase of In & Ge mixing during heating

(c) Crossection view of alloyed junction.

This process was used in the 1950 to produce diode and transistors. For example in the figure above, a sample of Ge crystal heated with a pellet of In on it.

Diffused junctions :- Diffused junctions are fabricated for IC technology purpose. In the IC fabrication technology - After CZ process a single crystal silicon is obtained in the form of cylinder as shown in the figure. we cut it in equal shap parts. Each part is circular and called Si-ware.

New wafer is pollished and d and



To make diffused junctions photolithography process used. photolithography process is a selective diffusion process to control junction Geometry.

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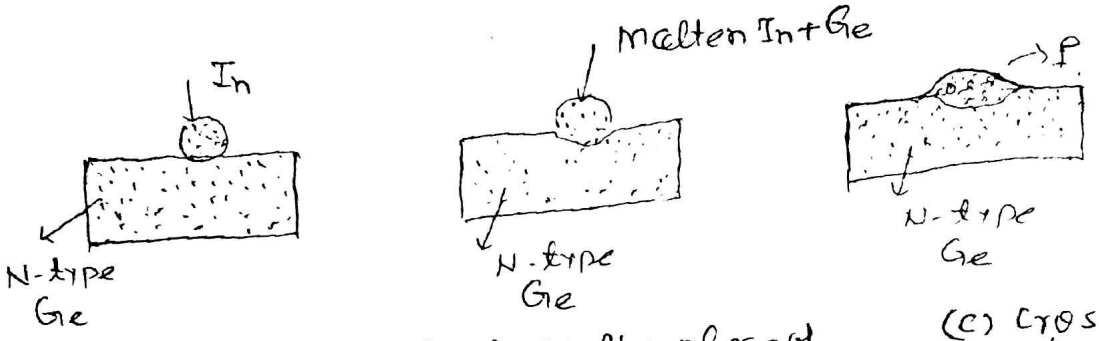

(a) Pellet of In in contact with n type Ge.

(b) Molten phase of In & Ge mixture during heating.

(c) Crossection view of alloyed junction.

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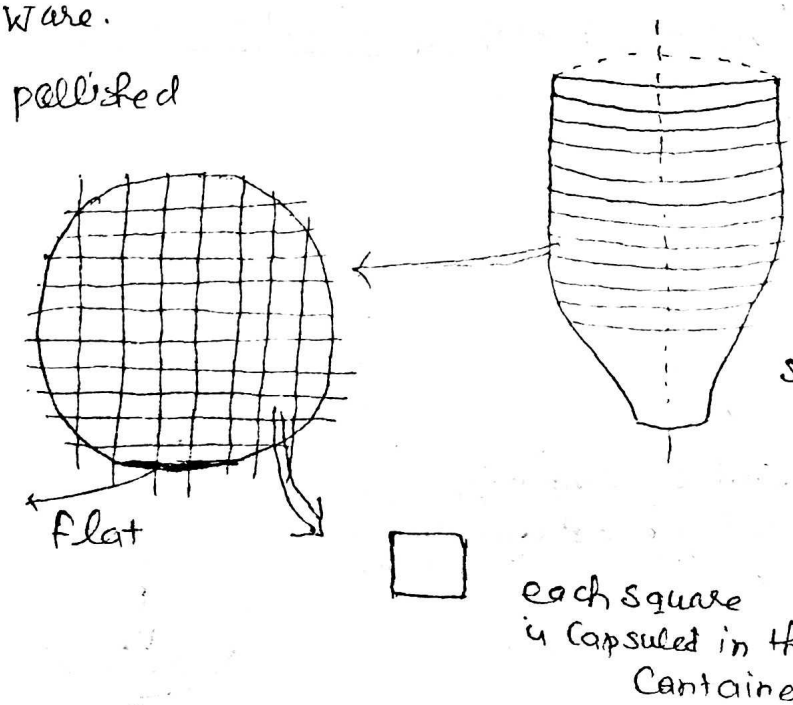
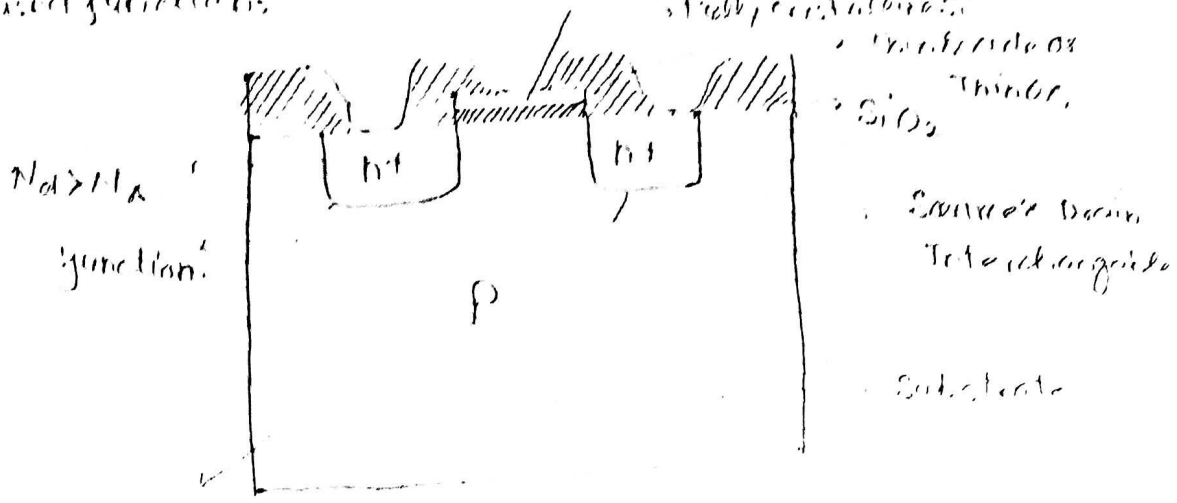


To make diffused junctions photolithography process is used. photolithography process is a selective diffusion process to control junction Geometry

figure shows structure of n-mos. where junction is not a diffused junction.

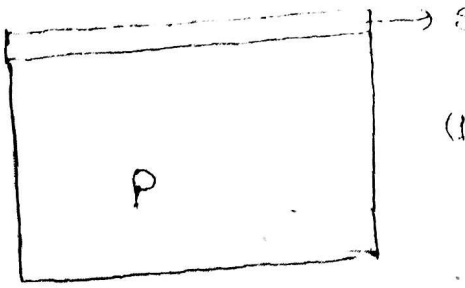


Structure of n-mos :-

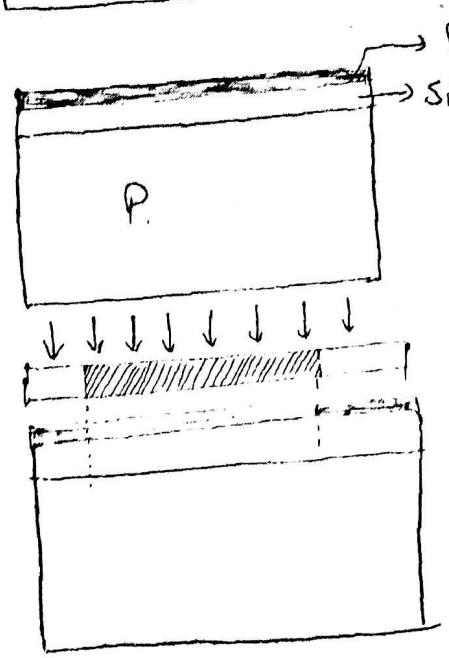
(actually cross section view of n-mos)

while 3 Dimentional view of n-mos is looking as usual.

Making a n-mos following steps are used -

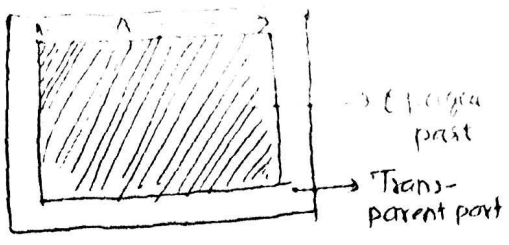


(1). Exicised Si Sample



(2):- Apply a layer of photoresist.

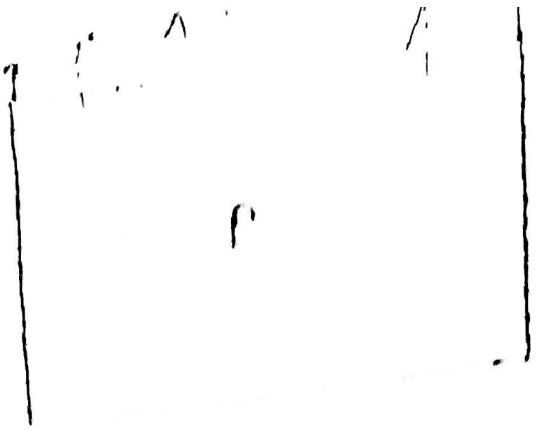
(3) :- Expose PR through photomask A.



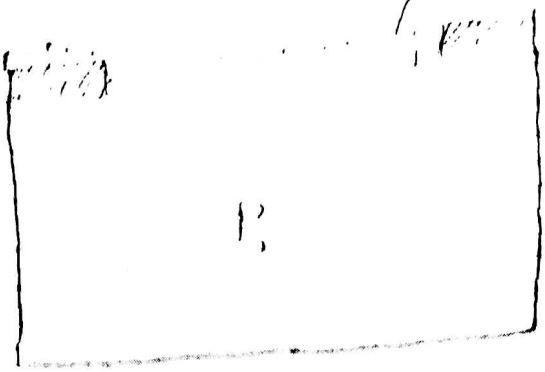
Glass photomask

→ (Top view of Glass photomask)

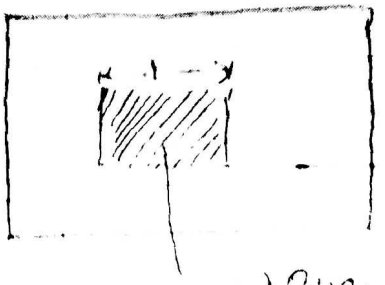
4. Opening of the window for diffusion.



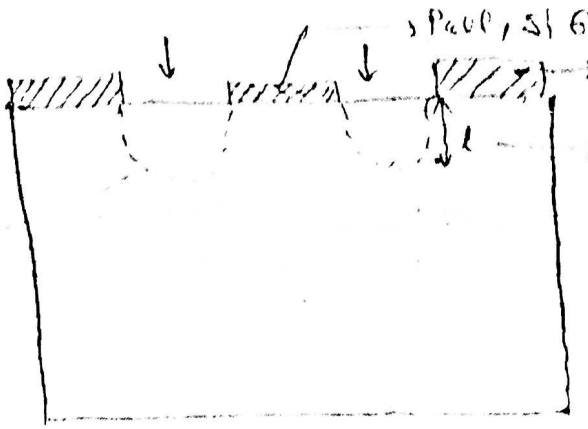
5. Poly silicon is deposited using chemical vapour deposition. Poly silicon is Gate layer.



6. After forming gate, again making Mask and repeat all previous steps again



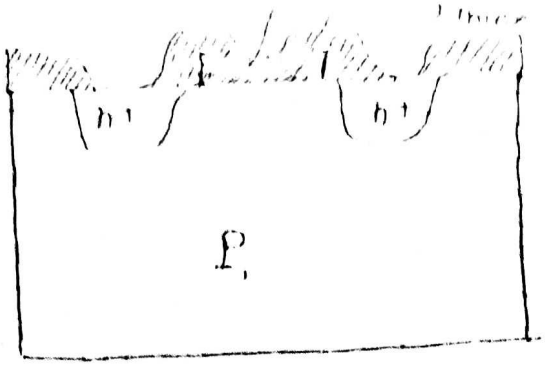
7.



Now these two windows ↓ ↓ are ready to make n+ region.

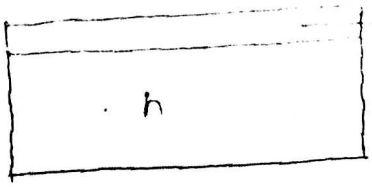
The depth of junction depends upon processing parameters → Diffusion time, Pressure, and other parameters.

→ For making n+ regions, ion implant is used.



Depletion type, n-MOS.

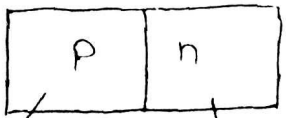
• Epitaxyle Junctions: Epitaxyl junctions are formed by using epitaxy process. In the epitaxy process an Layer is deposited by using, Chemical vapour deposition process. The epitaxyle layer some times called 'epi' Layer.



Epitaxyle junctions &
Alloyed junctions are modeled as ⇒ Step junction

⇓

Because there is Sharp 'P' region and 'n' region.



Left side only P-type. means acceptors

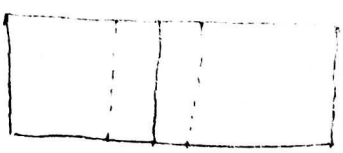
Right side only n-type.

Sharp junction.

On other Hand, diffused junctions are called ⇒ Graded junctions

Because.

Na - Nd varies across the junction.



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