Fault Models and design for Testability

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Fault Models

- The *fault* is the manifestation of manufacturing defects in an IC. During the IC fabrication, the MOS devices could be fabricated incorrectly, or the interconnect wires could have open-circuit or short-circuit fault.
- All these defects lead to malfunctioning of the IC. In order to differentiate good and bad chips, the faults must be identified in the bad chips.
- The fault models are used to identify different types of faults. There are many fault models.
- A list of fault models is shown in Table below

Fault Models

Sl. No.	Fault Model
1.	Physical fault
2.	Logical fault
3.	Degradation fault
4.	Parametric fault
5.	Timing or delay fault
6.	Open-circuit fault
7.	Short-circuit fault
8.	Stuck at fault
9.	Bridging fault

Fault Models

- A physical fault can be mapped to a logical fault. A fault can occur at two levels:
  - (a) chip level and
  - (b) device level.
- The logical faults can be classified into two main subclasses:
  - Degradation fault—this degrades the performance of the chip
  - Fatal fault—this causes the chip to malfunction
- The open-circuit and short-circuit faults are often grouped under fatal faults. A delay fault can be classified as a degradation fault, as it may not cause any functionality failure, but causes the chip to operate at a slower speed.

Fault Models

- The open-circuit fault is caused by several reasons. Some of the possible causes are as follows:
  - Bad contact
  - Over-etched metal
  - Break in poly silicon line
  - Void formed due to electromigration
- The short-circuit fault is also caused by various reasons. Some of the possible causes are as follows:
  - Under-etching of metal lines
  - Hillock formed due to electromigration
  - Junction spiking
  - Pinholes or shorts through the gate oxide
  - Diffusion shorts
- Another important fault is the bridging fault that happens in interconnects. It occurs mainly due to metal coverage problems.

Stuck at Fault

- The most popular fault model is the stuck-at fault model. In this model, there are two types of logical faults:
  - Stuck-at-1 (abbreviated as SA1 or S@1)
  - Stuck-at-0 (abbreviated as SA0 or S@0)
- The stuck-at-fault normally occurs due to the short circuit of the gate of the MOS device to either the *V*DD or to the ground and metal-to-metal shorts.
- The number of fault sites in a circuit is given by (Number of principal inputs + Number of gates + Number of fan-out branches). The number of single stuck at-fault is equal to twice the number of fault sites in the circuit.

Design for Testability

- A design is testable if it is controllable and observable. *Design for testability* (DFT) means the design must take into consideration the controllability and observability. The overhead of introducing the extra circuitry in the chip for DFT has a great impact on the cost of manufacturing test. It has a very good test coverage with a fewer number of test vectors.
- **Controllability**:While testing a circuit, it is often required to set a particular node to either logic 1 or logic 0. The nodes that are connected to the primary inputs are directly controllable. But it is not possible to set an internal node to a desired logic level directly. In such cases, it requires many test vectors to be applied to the primary inputs to set the node to a desired logic level. *Controllability* defines a measure of ease of setting an internal node logic level. It is the job of the chip designers to design the chip in such a way that all the nodes are easily controllable.
- ***Observability:***Similarly, any node that is connected directly to the primary output is easily observable. But for any internal node, it is not possible. The internal node logic level needs to be propagated to the primary outputs. *Observability* defines the degree at which the nodes are observed at the outputs. Again, good design practices are followed while doing the design to make a chip better observable.

Adhoc Testing

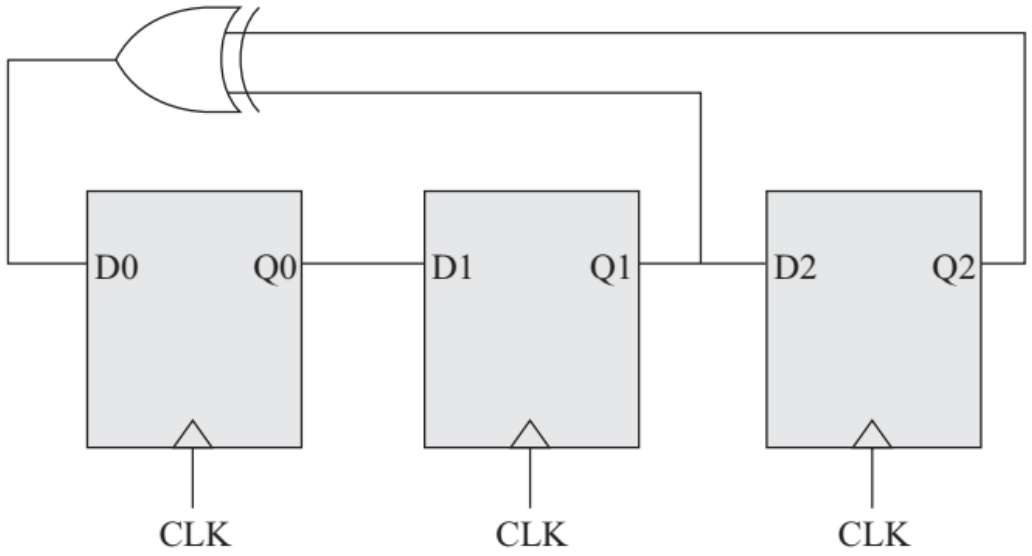
- The *ad hoc testing* is basically a combination of different simple test strategies that are used to reduce the number of tests from a large set of test patterns. It is suitable for small designs where the systematic test methodologies, e.g., scan test, ATPG, or BIST are not available. Following are the basic methods of ad hoc testing:
  - Large sequential circuits are partitioned into smaller ones.
  - Extra test points are added.
  - Multiplexers are added to multiplex the scan input and data input.
  - Easy state resets are provided.
- Though ad hoc testing is very effective, it depends on the architecture and requires expert knowledge. Hence, it is not very suitable for automation. The systematic and structured test methodologies are preferred over the ad hoc testing.

Built-in Self Test

- In built-in self test (BIST), a test logic circuit is incorporated in the chip. The extra circuit generates test patterns, applies them to the inputs, and tests the circuit. This extra circuit increases the chip size but reduces the test cycle time.
- The components of the BIST module are: (a) pseudo-random-sequence generator (PRSG) and (b) Signature analyzer
- **Linear Feedback Shift Register**
- The *linear feedback shift register* (LFSR) is used to generate pseudo-random test vectors in the chip. The outputs at each stage of an LFSR are used as the input of the circuit. The LFSR is clocked for a large number of cycles, and the output is monitored. A PRSG is a sequence of a particular length (n). The bit-pattern of the sequence is random in nature but has a periodicity. That is why it is called pseudorandom sequence. The sequence is constructed using D-flip-flops and a XOR gate.

Built-in Self Test

- An example of LFSR is shown in Fig.



A 3-bit LFSR

Built-in Self Test

- The length of the sequence is determined by the number of flip-flops (N) and is given by

$$n = 2^N - 1$$

- The states of the circuit, as shown in Fig. are shown in Table 14.4. It is assumed that initially, all the flip-flops are set to logic 1.
- The sequence generated by the circuit as shown in Fig. is 11100101. Note that the 000 state is not included in the LFSR states. If all zero states are included in a LFSR, it is known as complete feedback shift register (CFSR). CFSR is used in some special test situations.

Built-in Self Test

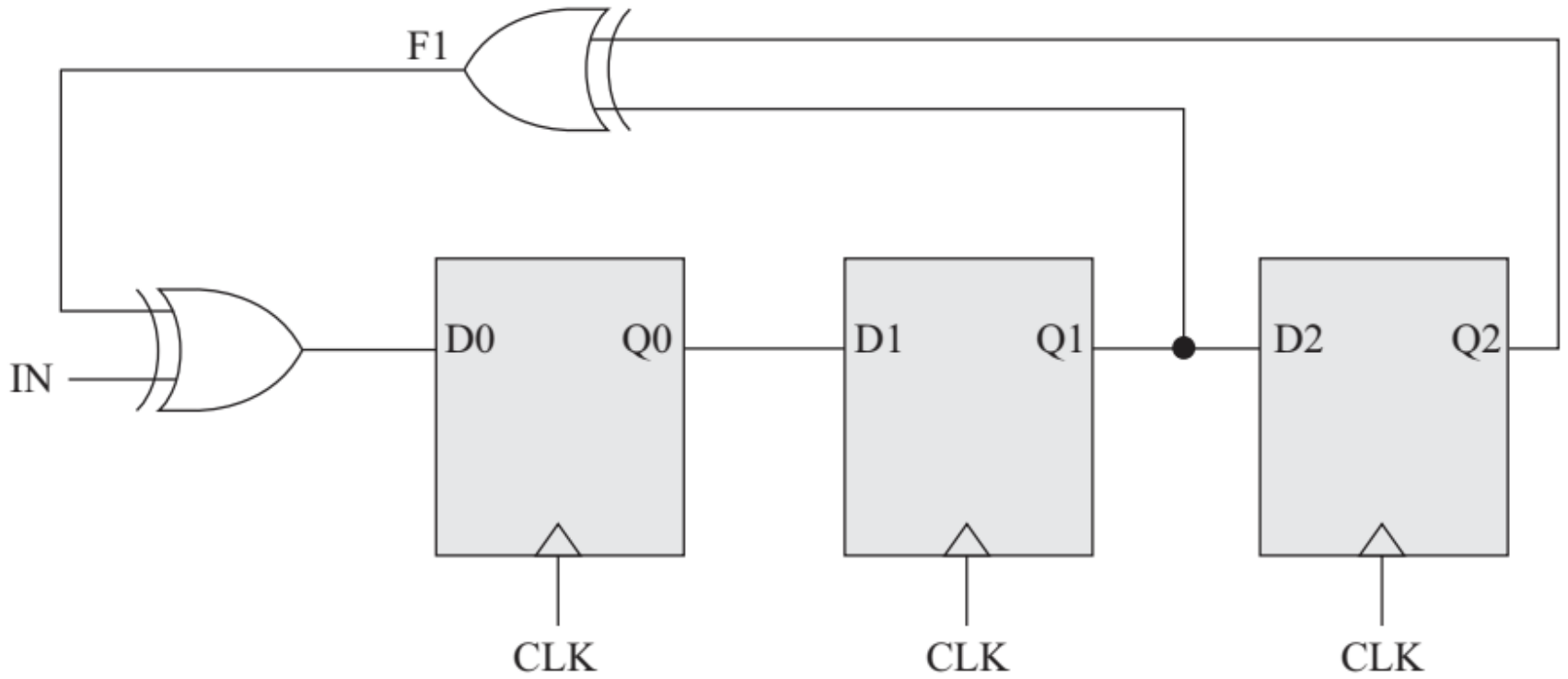
States of LFSR shown in Fig.

Clock pulse	Q0	Q1	Q2	Q0Q1Q2
1	1	1	1	111
2	0	1	1	011
3	0	0	1	001
4	1	0	0	100
5	0	1	0	010
6	1	0	1	101
7	1	1	0	110
8	1	1	1	111

Built-in Self Test

- **Signature Analyser**
- A *signature analyser* is formed by adding an extra XOR gate at the input of the LFSR, as shown in Fig. below. A binary input sequence is applied at the input IN. At the end of the input sequence, the shift register's output form a pattern. This pattern is known as a *signature*. A test input sequence is applied at the input, and the resulted output sequence is compared with the signature to determine a faulty circuit. If the length of the input sequence is long enough, it is unlikely that two different input sequences will produce the same signature. This test methodology is known as *signature analysis*.

Built-in Self Test



Signature analyser of LFSR shown in Fig. 14.6