Study material for

Course: Computer system Architechture Topic: Intel 8085 Microprocessor Sub Topic: Instruction set of Intel 8085 Microprocessor

Text Book Referred: Ramesh S. Gaonkar :Microprocessor Architechture, Programming, and Applications with the 8085, Fifth edition, Prentice Hall

Intel 8085 instruction set

The following abbreviation are used in the description of instruction set.

Flags.			Flace
Flags		c .	Flags
Reg. = 8085 register (B, C, D, E	:, H, L, A)	S	= sign
		Z	= zero
Mem = memory location (M) , If	the operand	AC	= Auxillary carry
is a Memory location, that is indic	ated by 16	Р	= Parity
bit address in HL register pair		CY	= Carry
Rs = Register source Rd =Register destination M = Memory () = content of		DE designated l	

SI. No.	opcode	operand	Description	Flags status after the instructio n execution	Example
1	ACI	8-bit data	Add Immediate to Accumulator with carry	All flags are modified to reflect the result of addition	ACI 57H H represents hexadecimal representation
2	ADC	Reg Mem.	Add operand (Register / memory) to accumulator with carry	All flags are modified to reflect the result of addition	ADC B ADC M

	1				1
3	ADD	Reg	Add Register or	All flags	ADD B
		Mem.	memory to	are	
			Accumulator	modified	ADD M
				to reflect	
				the result	
				of	
		0.1.1.		addition	
4	ADI	8 bit	Add Immediate to Accumulator	All flags	ADI 59H
		data	Accumulator	are modified	
				to reflect	
				the result	
				of	
				addition	
5	ANA	Pog	Logical AND with	S, Z, P are	ANA B
5	ANA	Reg Mem.	accumulator	modified	ANA M
		IVICIII.	accumulator	to reflect	
				the result	
				of	
				operation	
				. CY is	
				reset, AC	
				is set	
6	ANI	8 bit	AND immediate	S, Z, P are	ANI 34H
Ŭ		data	with accumulator	modified	
		uutu		to reflect	
				the result	
				of	
				operation	
				. CY is	
				reset, AC	
				is set	
7	CALL	16-bit	The program	No flags	CALL 2050H
	(unconditional	address	sequence is	are	
	subroutine call)		transferred to the	affected	
	There are some		address specified		
	conditional call		by the operand.		
	instructions also as		Before the transfer,		CC 2050H
	follows:		the address of the		CNC 2050H
	Flag status		next instruction to		CP 2050H
	CC : call on carry i.e CY=1		CALL (the content		CM 2050H
	CNC : call with no carry i.e CY=0 CP: call on positive i.e. S=0		of program		CPE 2050H
	CM: call on minus i.e. S=1		counter) is pushed		CPO 2050H
	CPE call on parity even i.e. P = 1 CPO: Call on parity odd i.e. P=0		on the stack		CZ 2050H
	CPO: Call on parity odd i.e. P=0 CZ: call on zero i.e Z=1				CNZ 2050H
	CNZ: call on no zero i.e. Z=0				
8	СМА	none	Complement	No flags	СМА
			accumulator	are	
				affected	
9	CMC	none	Complement carry	CY flag is	CMC
				modified,	

				No other	
				flags are	
10			a	affected	
10	CMP	Reg.	Compare with	S, P, AC	CMP B
		Mem.	accumulator . The	are also	CMP M
			comparison of two	modified	
			bytes is performed	in addition	
			by subtracting the	addition	
			content of operand from the content of	to Z and CY to	
			accumulator,	reflect	
			however neither	the result	
			contents are	of	
			modified	operation	
11	СРІ	8 bit	Compare	S, P, AC	СРІ В
1 11		data	Immediate with	are also	CPI M
		uuta	Accumulator.	modified	
			The second byte(8	in	
			bit data) with the	addition	
			content of	to Z and	
			accumulator.	CY to	
				reflect	
				the result	
				of	
				operation	
12	DAA	none	Decimal Adjust	S, Z, AC,	DAA
			Accumulator'	P, CY flags	
			The content of	are	
			accumulator is	affected	
			changed from a	reflect	
			binary value to two	the result	
			4 bit Binary Coded	of	
			Decimal(BCD)	operation	
13	DAD	Reg.	Add register pair to	If the	DAD H
		pair	H and L registers	result is	(multiply the
				larger	content of HL
				than 16	register pair by 2)
				bit, CY is	
				set. No	DAD B
				other	
				flags are	
			Deserves	affected	DCDD
14	DCR	REG.	Decrement source	S, Z, P, AC	DCR B
		Mem.	by 1	are	DCDM
				modified	DCR M
				to reflect	
				the result of	
				operation . CY is not	
				modified	
L	1		1	mounieu	

15	DCY	Doc	Dooron ont resister	Noffers	
15	DCX	Reg.	Decrement register	No flags	DCX D
		pair	pair by 1	are	
<u> </u>				affected	
16	DI	None	Disable Interrupts	No flags	DI
			(Interrupt enable	are	
			flip-flop is reset	affected	
			and all interrupts		
			except the TRAP		
			are disabled		
17	EI	None	Enable Interrupts	No flags	EI
			(Interrupt enable	are	
			flip-flop is reset	affected	
			and all interrupts		
			(except TRAP) are		
			enabled		
18	HLT	None	Halt and enter wait	No flags	HLT
			state	are	
				affected	
19	IN	8-bit	Input data to	No flags	IN 23H
1		port	accumulator from a	are	114 2011
		address		affected	
		auuress	port with 8-bit	anecteu	
20	IND	Dec	address		
20	INR	Reg.	Increment contents	S, Z, P, AC	INR B
		Mem.	of register/	are	
			Memory by 1	modified	INR M
				to reflect	
				the result	
				of	
				operation	
				. CY is not	
				modified	
21	INX	Reg.	Increment Register	No flags	INX H
		pair	pair by 1	are	Content of entire
				affected	HL register pair is
					incremented by 1
22	JMP	16-bit	Jump	No flags	
		address	Unconditionally (are	
		4441 (33	the program	affected	
	There are some		sequence is	unceleu	
	conditional call		transferred to		
	instructions also as		memory location		
	follows:		specified by the 16		
	Flag status JC : call on carry i.e CY=1		bit address)		
	JC : call on carry i.e CY=1 JNC : call with no carry i.e CY=0				
	JP: call on positive i.e. S=0				
	JM: call on minus i.e. S=1				
	JPE call on parity even i.e. P = 1 JPO: Call on parity odd i.e. P=0				
	JZ: call on zero i.e Z=1				
	JNZ: call on no zero i.e. Z=0				

23	LDA	16-bit	Load Accumulator	No flags	LDA 2050H
		address	Direct	are	203011
				affected	
24	LDAX	B/D Reg.	Load Accumulator	No flags	LDAX B
		Pair	Indirect	are	
			mancet	affected	
25	LHLD	16-bit	Load H and L	No flags	LHLD 2050H
		address	registers Direct	are	
		auuress	Tegisters Direct	affected	
26	LXI	Reg. pair ,	Load Register pair	No flags	LXI B, 2050H
10		16 bit	Immediate	are	LAI B, 2030H
		address	IIIIIIeulate	affected	
7	MOV	Dd Dc	Mova Convitrom		
27	MOV	Rd,Rs	Move- Copy from	No flags	MOV B, C
		M,Rs	Source to	are	MOV M, B
	D (1) (1	Rd,M	Destination	affected	MOV B, M
28	MVI	Reg., data Mem., Data	Move Immediate 8-	No flags	MVI B, 92H
		,	bit	are	MVI M, 3AH
				affected	
29	NOP	None	No Operation	No flags	NOP
			(No peration is	are	
			performed. Only	affected	
			Fetch and decoded,		
			however used to fill		
			the delays and		
			insert instructions		
			while		
			troubleshooting)		
30	ORA	Reg.	Logically OR with	S, Z, P are	ORA C
		Mem.	accumulator	modified	
				to reflect	
				the result	
					1
				of	
				of operation	
				operation	
31	ORI	8 bit	Logically OR	operation . AC, CY	ORI 56H
31	ORI	8 bit data	Logically OR Immediate with	operation . AC, CY are reset	ORI 56H
31	ORI			operation . AC, CY are reset S, Z, P are	ORI 56H
31	ORI		Immediate with	operation . AC, CY are reset S, Z, P are modified	ORI 56H
31	ORI		Immediate with	operation . AC, CY are reset S, Z, P are modified to reflect	ORI 56H
31	ORI		Immediate with	operation . AC, CY are reset S, Z, P are modified to reflect the result	ORI 56H
31	ORI		Immediate with	operation . AC, CY are reset S, Z, P are modified to reflect the result of operation	ORI 56H
31	ORI		Immediate with	operation . AC, CY are reset S, Z, P are modified to reflect the result of operation . AC, CY	ORI 56H
31		data	Immediate with accumulator	operation . AC, CY are reset S, Z, P are modified to reflect the result of operation . AC, CY are reset	
	ORI	data 8-bit	Immediate with accumulator Output data from	operation . AC, CY are reset S, Z, P are modified to reflect the result of operation . AC, CY are reset No flags	ORI 56H OUT 11H
		data 8-bit port	Immediate with accumulator Output data from accumulator to a	operation . AC, CY are reset S, Z, P are modified to reflect the result of operation . AC, CY are reset No flags are	
		data 8-bit	Immediate with accumulator Output data from accumulator to a port with 8-bit	operation . AC, CY are reset S, Z, P are modified to reflect the result of operation . AC, CY are reset No flags	
32	OUT	data 8-bit port address	Immediate with accumulator Output data from accumulator to a port with 8-bit address	operation . AC, CY are reset S, Z, P are modified to reflect the result of operation . AC, CY are reset No flags are affected	OUT 11H
		data 8-bit port	Immediate with accumulator Output data from accumulator to a port with 8-bit	operation . AC, CY are reset S, Z, P are modified to reflect the result of operation . AC, CY are reset No flags are	

34	РОР	Reg.pair	POP off stack to	No flags	POP H
54		Neg.pan	register pair	are	r Or II
			(B/D/H/PSW)	affected	
35	PUSH	Reg.pair	PUSh register pair	No flags	PUSH H
55	rosii	Neg.pan	(B/D/H/PSW) on to	are	rosiin
			stack	affected	
36	RAL	None	Rotate	CY is	RAL
50	NAL	None	Accumulator Left	modified	NAL
			through Carry	according	
			through Carry	to bit D7.	
				S,Z,AC, P	
				are not	
				affected	
27	DAD	None	Detete		
37	RAR	None	Rotate	CY is	RAR
			Accumulator Right	modified	
			through Carry	according	
				to bit DO.	
				S,Z,AC, P	
				are not	
20	RLC	Nees	Detete	affected	DLC.
38	RLC	None	Rotate	CY is	RLC
			Accumulator Left	modified	
				according	
				to bit D7.	
				S,Z,AC, P	
				are not	
20	DDC	Nama	Datata	affected	DAL
39	RRC	None	Rotate	CY is	RAL
			Accumulator Right	modified	
				according	
				to bit D0.	
				S,Z,AC, P	
				are not affected	
40	DET	None	Boturn from		DET
40	RET	None	Return from	No flags	RET
	There are some		Subroutine	are	
	conditional Return		unconditionally	affected	
	instructions also as				
	follows:				
	Flag status RC : return on carry i.e CY=1				
	RNC : return with no carry i.e				
	CY=0				
	RP: return on positive i.e. S=0 RM: return on minus i.e. S=1				
	RPE return I on parity even i.e. P				
	= 1 PPO: roturn on parity odd i o P=0				
	RPO: return on parity odd i.e. P=0 RZ: return on zero i.e Z=1				
	RNZ: call on no zero i.e. Z=0				
41	RIM	None	Read Interrupt	No flags	RIM
			Mask	are	
				affected	

42	RST	0/1/2/3 /4/5/6/ 7	Restart	No flags are affected	Opcode/operand and restart address RST 0 0000H RST 1 0008H RST 2 0010H RST3 0018H RST 4 0020H RST 5 0028H RST 6 0030H RST 7 0038H
43	SBB	Reg. Mem.	Subtract Source and Borrow from Accumulator	All flags are altered to reflect the result of the subtraction	SBB B
44	SBI	8 bit data	Subtract Immediate with Borrow	All flags are altered to reflect the result of the subtraction	SBI 23H
45	SHLD	16 bit address	Store H and L registers Direct	No flags are affected	SHLD 2050H
46	SIM	None	Set Interrupt Mask	No flags are affected	SIM
47	SPHL	None	Copy H and L Registers to Stack Pointer	No flags are affected	SPHL
48	STA	16 bit address	Store Accumulator Direct	No flags are affected	STA 2050 H
49	STAX	B/D reg. pair	Store Accumulator Indirect	No flags are affected	STAX B STAX D
50	STC	None	Set Carry	The carry flag is set to 1	STC
51	SUB	Reg Mem.	Sub Register or memory from Accumulator: results are placed in accumulator	All flags are modified to reflect the result of subtraction	SUB B SUB M
52	SUI	8 bit data	Sub 8 bit data from Accumulator : results are placed in accumulator	All flags are modified to reflect the result of subtraction	SUI 23H
53	XCHG	None	Exchange H and L with D and E	No flags are affected	XCHG
54	XRA	Reg. Mem.	Exclusive OR with Accumulator	S, Z, P are modified to reflect the result of operation. AC, CY are reset	XRA D XRA M

55	XRI	8 bit data	Exclusive OR Immediate with Accumulator	S, Z, P are modified to reflect the result of operation. AC, CY are reset	XRI 34H
56	XTHL	None	Exchange h and L with Top of Stack	No flags are affected	XTHL