Study material for

Course: Computer system Architechture

Topic: Intel 8085 Microprocessor

Sub Topic: Instruction set of Intel 8085 Microprocessor

Text Book Referred: Ramesh S. Gaonkar :Microprocessor Architechture, Programming, and Applications with the 8085, Fifth edition , Prentice Hall

Intel 8085 instruction set

The following abbreviation are used in the description of instruction set.

Flags Reg. = 8085 register (B, C, D, E, H, L, A) Mem = memory location (M) , If the operand is a Memory location, that is indicated by 16 bit address in HL register pair Rs = Register source Rd =Register destination M = Memory ( ) = content of	**Flags** S = sign Z = zero AC = Auxillary carry P = Parity CY = Carry SP represents Stack Pointer PSW represents for Accumulator and flag register pair Reg. pair BC designated by B in the instruction DE designated by D in the instruction HL designated by H in the instruction

Sl. No.	opcode	operand	Description	Flags status after the instruction execution	Example
1	ACI	8-bit data	Add Immediate to Accumulator with carry	All flags are modified to reflect the result of addition	ACI 57H H represents hexadecimal representation
2	ADC	Reg Mem.	Add operand (Register / memory) to accumulator with carry	All flags are modified to reflect the result of addition	ADC B ADC M

3	ADD	Reg Mem.	Add Register or memory to Accumulator	All flags are modified to reflect the result of addition	ADD B ADD M
4	ADI	8 bit data	Add Immediate to Accumulator	All flags are modified to reflect the result of addition	ADI 59H
5	ANA	Reg Mem.	Logical AND with accumulator	S, Z, P are modified to reflect the result of operation . CY is reset, AC is set	ANA B ANA M
6	ANI	8 bit data	AND immediate with accumulator	S, Z, P are modified to reflect the result of operation . CY is reset, AC is set	ANI 34H
7	CALL (unconditional subroutine call) There are some conditional call instructions also as follows: **Flag status** CC : call on carry i.e CY=1 CNC : call with no carry i.e CY=0 CP: call on positive i.e. S=0 CM: call on minus i.e. S=1 CPE call on parity even i.e. P = 1 CPO: Call on parity odd i.e. P=0 CZ: call on zero i.e Z=1 CNZ: call on no zero i.e. Z=0	16-bit address	The program sequence is transferred to the address specified by the operand. Before the transfer, the address of the next instruction to CALL (the content of program counter) is pushed on the stack	No flags are affected	CALL 2050H CC 2050H CNC 2050H CP 2050H CM 2050H CPE 2050H CPO 2050H CZ 2050H CNZ 2050H
8	CMA	none	Complement accumulator	No flags are affected	CMA
9	CMC	none	Complement carry	CY flag is modified ,	CMC

				No other flags are affected	
10	CMP	Reg. Mem.	Compare with accumulator . The comparison of two bytes is performed by subtracting the content of operand from the content of accumulator, however neither contents are modified	S, P, AC are also modified in addition to Z and CY to reflect the result of operation	CMP B CMP M
11	CPI	8 bit data	Compare Immediate with Accumulator. The second byte(8 bit data)with the content of accumulator.	S, P, AC are also modified in addition to Z and CY to reflect the result of operation	CPI B CPI M
12	DAA	none	Decimal Adjust Accumulator' The content of accumulator is changed from a binary value to two 4 bit Binary Coded Decimal(BCD)	S, Z, AC, P, CY flags are affected reflect the result of operation	DAA
13	DAD	Reg. pair	Add register pair to H and L registers	If the result is larger than 16 bit, CY is set. No other flags are affected	DAD H (multiply the content of HL register pair by 2) DAD B
14	DCR	REG. Mem.	Decrement source by 1	S, Z, P, AC are modified to reflect the result of operation . CY is not modified	DCR B DCR M

15	DCX	Reg. pair	Decrement register pair by 1	No flags are affected	DCX D
16	DI	None	Disable Interrupts (Interrupt enable flip-flop is reset and all interrupts except the TRAP are disabled	No flags are affected	DI
17	EI	None	Enable Interrupts (Interrupt enable flip-flop is reset and all interrupts (except TRAP) are enabled	No flags are affected	EI
18	HLT	None	Halt and enter wait state	No flags are affected	HLT
19	IN	8-bit port address	Input data to accumulator from a port with 8-bit address	No flags are affected	IN 23H
20	INR	Reg. Mem.	Increment contents of register/ Memory by 1	S, Z, P, AC are modified to reflect the result of operation . CY is not modified	INR B INR M
21	INX	Reg. pair	Increment Register pair by 1	No flags are affected	INX H Content of entire HL register pair is incremented by 1
22	JMP There are some conditional call instructions also as follows: **Flag status** JC : call on carry i.e CY=1 JNC : call with no carry i.e CY=0 JP: call on positive i.e. S=0 JM: call on minus i.e. S=1 JPE call on parity even i.e. P = 1 JPO: Call on parity odd i.e. P=0 JZ: call on zero i.e Z=1 JNZ: call on no zero i.e. Z=0	16-bit address	Jump Unconditionally (the program sequence is transferred to memory location specified by the 16 bit address)	No flags are affected	

23	LDA	16-bit address	Load Accumulator Direct	No flags are affected	LDA 2050H
24	LDAX	B/D Reg. Pair	Load Accumulator Indirect	No flags are affected	LDAX B
25	LHLD	16-bit address	Load H and L registers Direct	No flags are affected	LHLD 2050H
26	LXI	Reg. pair , 16 bit address	Load Register pair Immediate	No flags are affected	LXI B, 2050H

27	MOV	Rd,Rs
		M,Rs
		Rd,M
			Move- Copy from Source to Destination	No flags are affected	MOV B, C
					MOV M, B
					MOV B, M

28	MVI	Reg., data Mem., Data	Move Immediate 8-bit	No flags are affected	MVI B, 92H MVI M, 3AH
29	NOP	None	No Operation (No peration is performed. Only Fetch and decoded, however used to fill the delays and insert instructions while troubleshooting)	No flags are affected	NOP
30	ORA	Reg. Mem.	Logically OR with accumulator	S, Z, P are modified to reflect the result of operation . AC, CY are reset	ORA C
31	ORI	8 bit data	Logically OR Immediate with accumulator	S, Z, P are modified to reflect the result of operation . AC, CY are reset	ORI 56H
32	OUT	8-bit port address	Output data from accumulator to a port with 8-bit address	No flags are affected	OUT 11H
33	PCHL	None	Load Program Counter With HL Content	No flags are affected	PCHL

34	POP	Reg.pair	POP off stack to register pair (B/D/H/PSW)	No flags are affected	POP H
35	PUSH	Reg.pair	PUSh register pair (B/D/H/PSW) on to stack	No flags are affected	PUSH H
36	RAL	None	Rotate Accumulator Left through Carry	CY is modified according to bit D7. S,Z,AC, P are not affected	RAL
37	RAR	None	Rotate Accumulator Right through Carry	CY is modified according to bit D0. S,Z,AC, P are not affected	RAR
38	RLC	None	Rotate Accumulator Left	CY is modified according to bit D7. S,Z,AC, P are not affected	RLC
39	RRC	None	Rotate Accumulator Right	CY is modified according to bit D0. S,Z,AC, P are not affected	RAL
40	RET There are some conditional Return instructions also as follows: **Flag status** RC : return on carry i.e CY=1 RNC : return with no carry i.e CY=0 RP: return on positive i.e. S=0 RM: return on minus i.e. S=1 RPE return l on parity even i.e. P = 1 RPO: return on parity odd i.e. P=0 RZ: return on zero i.e Z=1 RNZ: call on no zero i.e. Z=0	None	Return from Subroutine unconditionally	No flags are affected	RET
41	RIM	None	Read Interrupt Mask	No flags are affected	RIM

42	RST	0/1/2/3/4/5/6/7	Restart	No flags are affected	**Opcode/operand** and **restart address** **RST 0 0000H** **RST 1 0008H** **RST 2 0010H** **RST3 0018H** **RST 4 0020H** **RST 5 0028H** **RST 6 0030H** **RST 7 0038H**
43	SBB	Reg. Mem.	Subtract Source and Borrow from Accumulator	All flags are altered to reflect the result of the subtraction	SBB B
44	SBI	8 bit data	Subtract Immediate with Borrow	All flags are altered to reflect the result of the subtraction	SBI 23H
45	SHLD	16 bit address	Store H and L registers Direct	No flags are affected	SHLD 2050H
46	SIM	None	Set Interrupt Mask	No flags are affected	SIM
47	SPHL	None	Copy H and L Registers to Stack Pointer	No flags are affected	SPHL
48	STA	16 bit address	Store Accumulator Direct	No flags are affected	STA 2050 H
49	STAX	B/D reg. pair	Store Accumulator Indirect	No flags are affected	STAX B STAX D
50	STC	None	Set Carry	The carry flag is set to 1	STC
51	SUB	Reg Mem.	Sub Register or memory from Accumulator: results are placed in accumulator	All flags are modified to reflect the result of subtraction	SUB B SUB M
52	SUI	8 bit data	Sub 8 bit data from Accumulator : results are placed in accumulator	All flags are modified to reflect the result of subtraction	SUI 23H
53	XCHG	None	Exchange H and L with D and E	No flags are affected	XCHG
54	XRA	Reg. Mem.	Exclusive OR with Accumulator	S, Z, P are modified to reflect the result of operation. AC, CY are reset	XRA D XRA M

55	XRI	8 bit data	Exclusive OR Immediate with Accumulator	S, Z, P are modified to reflect the result of operation. AC, CY are reset	XRI 34H
56	XTHL	None	Exchange h and L with Top of Stack	No flags are affected	XTHL