MOS Circuit Design

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MOS layers

- MOS circuits are formed on four basic layers
  - N-diffusion
  - P-diffusion
  - Polysilicon
  - Metal

Which are isolated by thick or thin silicon dioxide insulating layer

- There should be way of capturing the topology and layer information of the actual circuit in silicon so that we can set out simple diagrms which convey both layer information topology.

Stick diagram

- VLSI design aims to translate circuit concepts onto silicon.
- Stick diagrams are a means of capturing topography and layer information using simple diagrams.
- Stick diagrams convey layer information through color codes (or monochrome encoding).
- Acts as an interface between symbolic circuit and the actual layout.

Stick diagram

- Stick diagram may be used to convey layer information through the use of colour codes, for example in case of nMOS design
  - Red for polysilicon
  - Blue for metal
  - Yellow for implant
  - **Black** for contact areas

Stick diagram

- Does ***not*** show
  - Exact placement of components
  - Transistor sizes
  - Wire lengths, wire widths, tub boundaries
  - Any other low level details such as parasitics

Stick Diagrams – Notations

Can also draw in shades of gray/line style.

Buried Contact

Contact Cut

ENCODING FOR SINGLE METAL NMOS PROCESS

COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING
GREEN		n-diffusion (n+ active) Thinox*	 *Thinox = n-diff. + transistor channels
RED		Polysilicon	
BLUE		Metal 1	
BLACK		Contact cut	
GRAY	NOT APPLICABLE	Overglass	
nMOS ONLY YELLOW		Implant	
nMOS ONLY BROWN		Buried contact	

Stick Diagrams – Some Rules

Rule 1:

When two or more 'sticks' of the same type cross or touch each other that represents electrical contact.

Stick Diagrams – Some Rules

Rule 2:

When two or more 'sticks' of different type cross or touch each other there is no electrical contact.

(If electrical contact is needed we have to show the connection explicitly)

Stick Diagrams – Some Rules

Rule 3:

When a poly crosses diffusion it represents a transistor.

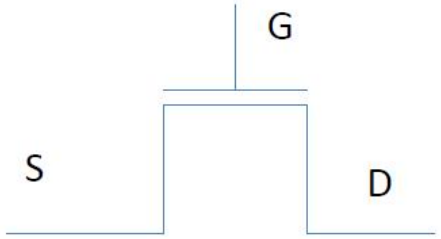
Note: If a contact is shown then it is ***not*** a transistor.

Stick Diagrams – Some Rules

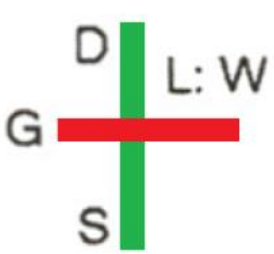
Rule 4:

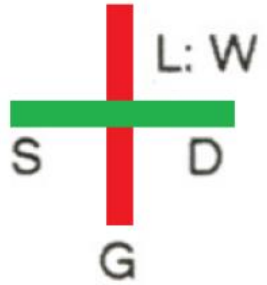
In CMOS a demarcation line is drawn to avoid touching of p-diff with n-diff. All PMOS must lie on one side of the line and all NMOS will have to be on the other side.

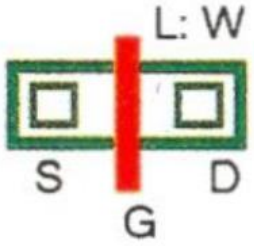
N type enhancement mode transistor



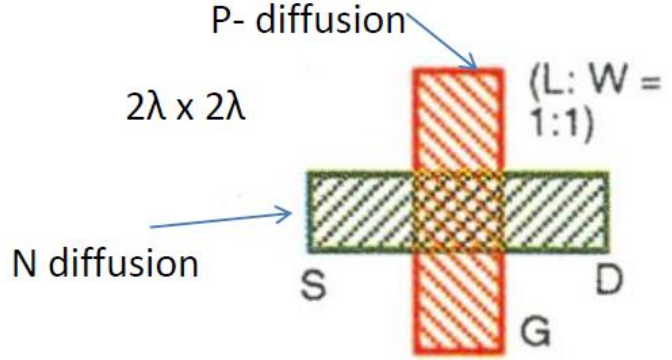
STICK DIAGRAM





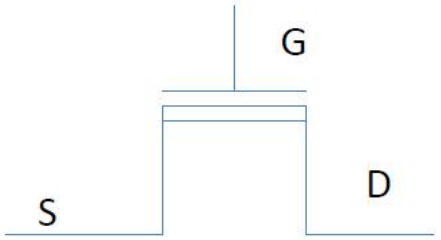


SYMBOL



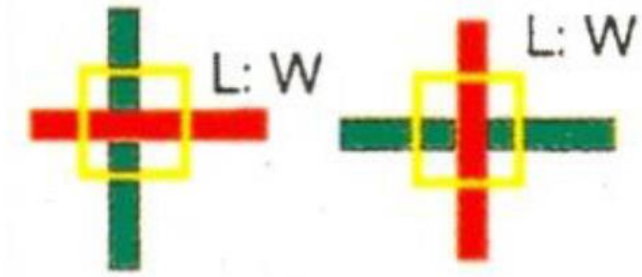
MASK LAYOUT

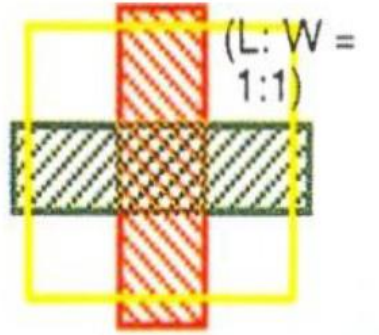
N type depletion mode transistor



SYMBOL

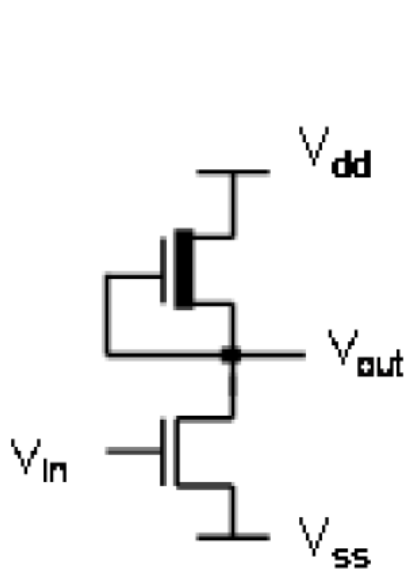
STICK DIAGRAM



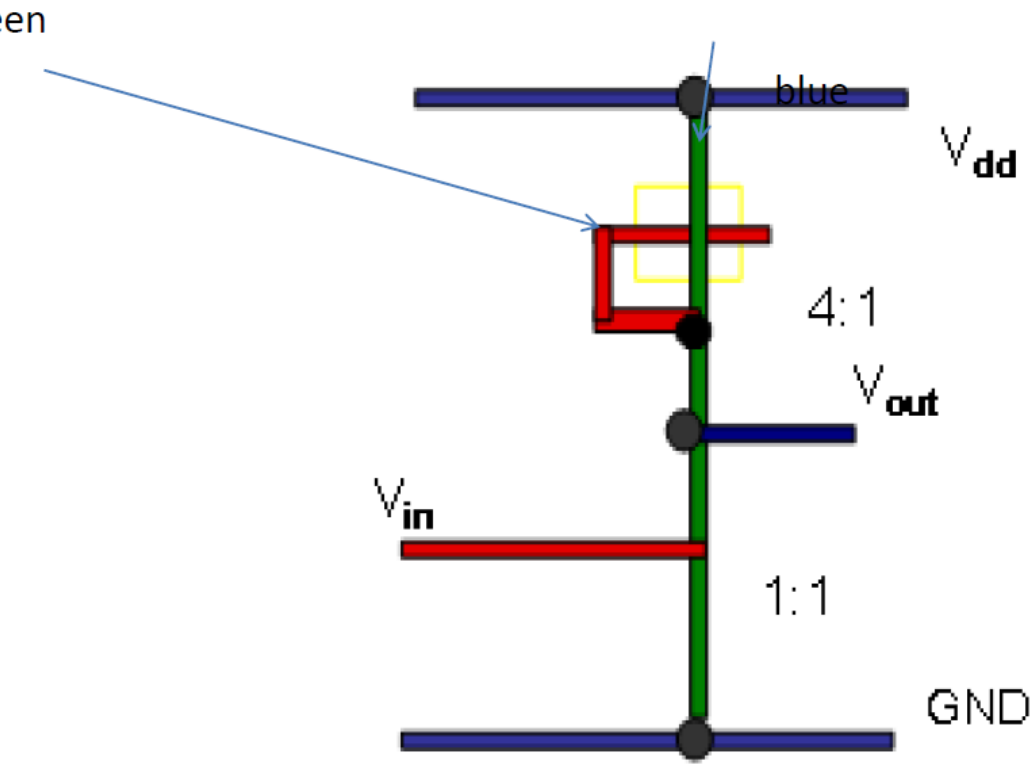


MASK LAYOUT

nMOS depletion load inverter

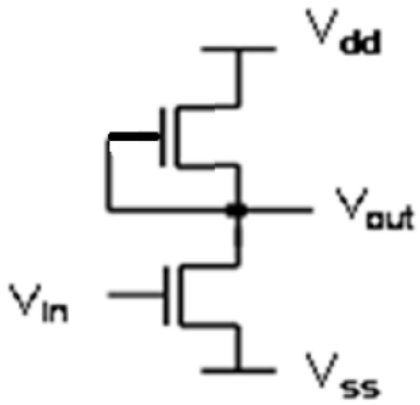


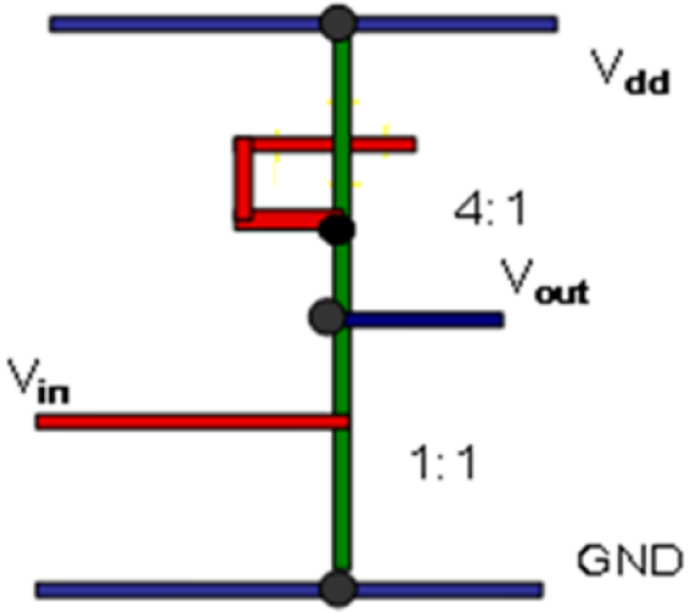
Schematic



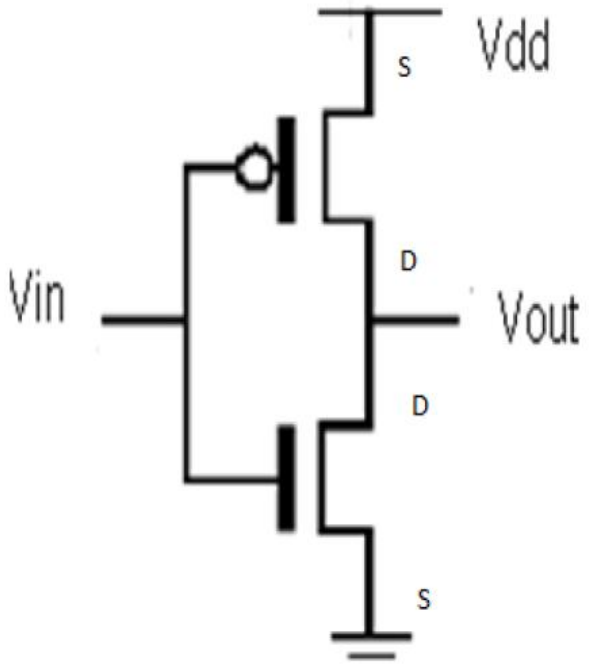
Stick diagram

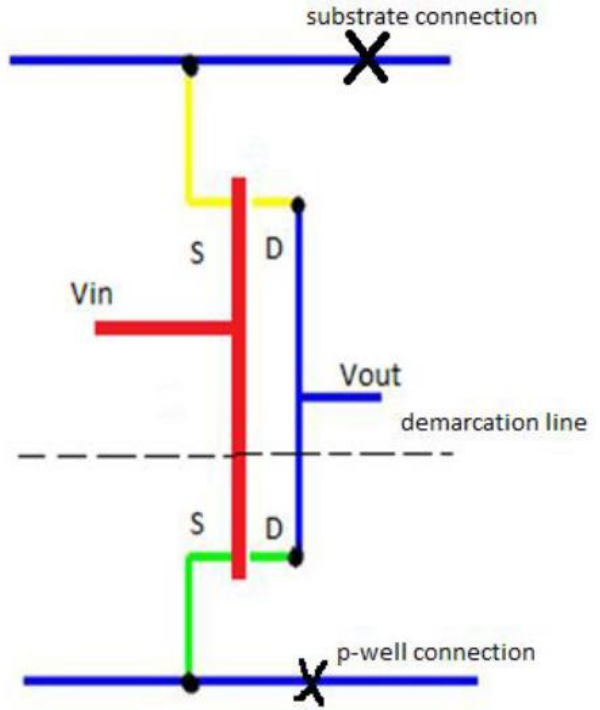
nMOS enhancement load inverter





CMOS INVERTER





DESIGN RULES

- **Why we use design rules?**
  - Interface between designer and process engineer

- Historically, the process technology referred to the length of the silicon channel between the source and drain terminals in field effect transistors.
- The sizes of other features are generally derived as a ratio of the channel length, where some may be larger than the channel size and some smaller.
  - For example, in a 90 nm process, the length of the channel may be 90 nm, but the width of the gate terminal may be only 50 nm.

DESIGN RULES

Semiconductor manufacturing processes

- 10 µm — 1971
- 3 µm — 1975
- 1.5 µm — 1982
- 1 µm — 1985
- 800 nm (0.80 µm) — 1989
- 600 nm (0.60 µm) — 1994
- 350 nm (0.35 µm) — 1995
- 250 nm (0.25 µm) — 1998
- **180 nm** (0.18 µm) — 1999
- 130 nm (0.13 µm) — 2000
- 90 nm — 2002
- 65 nm — 2006
- 45 nm — 2008
- 32 nm — 2010
- 22 nm — approx. 2011
- 16 nm — approx. 2018
- 11 nm — approx. 2022

DESIGN RULES

- Allow translation of circuits (usually in stick diagram or symbolic form) into actual geometry in silicon
- Interface between circuit designer and fabrication engineer
- Compromise
  - designer - tighter, smaller
  - fabricator - controllable, reproducible

DESIGN RULES

- Design rules define ranges for features
  - Examples:
    - min. wire widths to avoid breaks
    - min. spacing to avoid shorts
    - minimum overlaps to ensure complete overlaps
  - Measured in microns
  - Required for resolution/tolerances of masks

- Fabrication processes defined by minimum channel width
  - Also minimum width of poly traces
  - Defines “how fast” a fabrication process is

DESIGN RULES

- **Two major approaches:**
  - **"Micron" rules: stated at micron resolution.**
  - **λ rules: simplified micron rules with limited scaling attributes.**
- **Design rules represents a tolerance which insures very high probability of correct fabrication**
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)

DESIGN RULES

"Micron" rules

- All minimum sizes and spacing specified in microns.
- Rules don't have to be multiples of λ.
- Can result in 50% reduction in area over λ based rules
- Standard in industry.

DESIGN RULES

Lambda-based Design Rules

- *Lambda-based* (scalable CMOS) design rules define scalable rules based on λ (which is half of the minimum channel length)
  - classes of MOSIS SCMOS rules: SUBMICRON, DEEPSUBMICRON
- Stick diagram is a draft of real layout, it serves as an abstract view between the schematic and layout.

DESIGN RULES

Lambda-based Design Rules

- Circuit designer in general want tighter, smaller layouts for improved performance and decreased silicon area.
- On the other hand, the process engineer wants design rules that result in a controllable and reproducible process.
- Generally we find there has to be a compromise for a competitive circuit to be produced at a reasonable cost.
- All widths, spacing, and distances are written in the form
- $\lambda = 0.5$ X minimum drawn transistor length

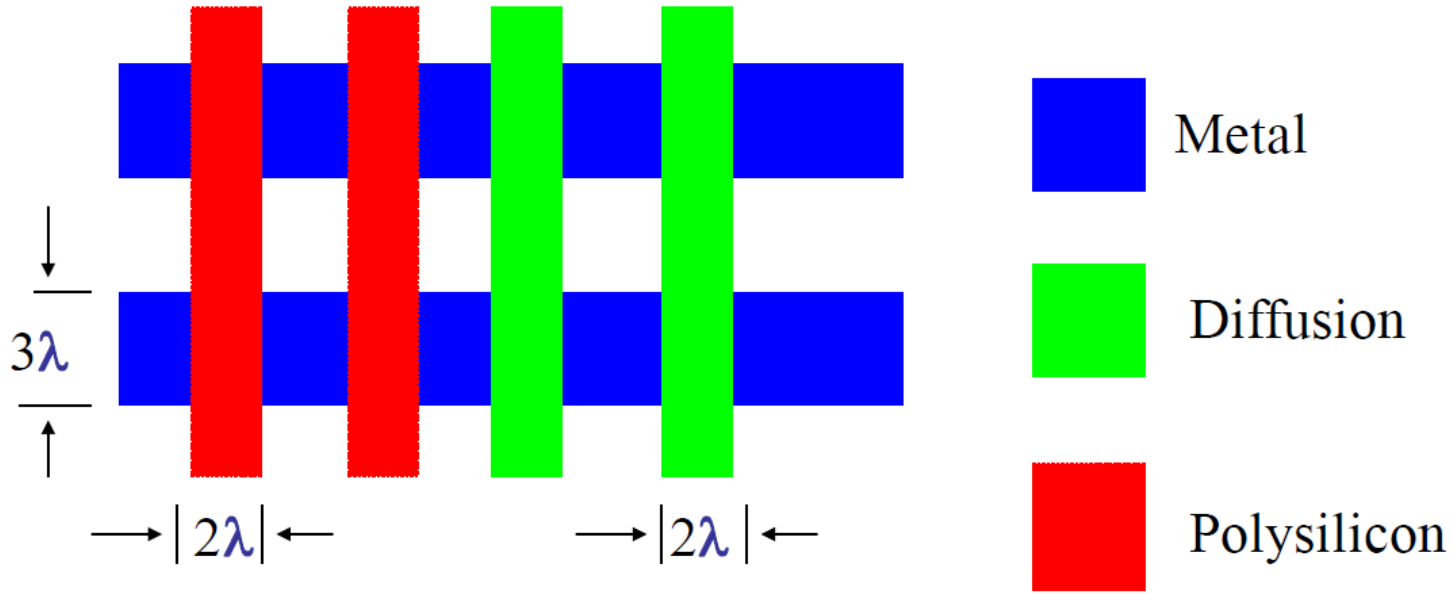
DESIGN RULES

Lambda-based Design Rules

- Design rules based on single parameter, λ
- Simple for the designer
- Wide acceptance
- Provide feature size independent way of setting out mask
- If design rules are obeyed, masks will produce working circuits
- Minimum feature size is defined as 2 λ
- Used to preserve topological features on a chip
- Prevents shorting, opens, contacts from slipping out of area to be contacted

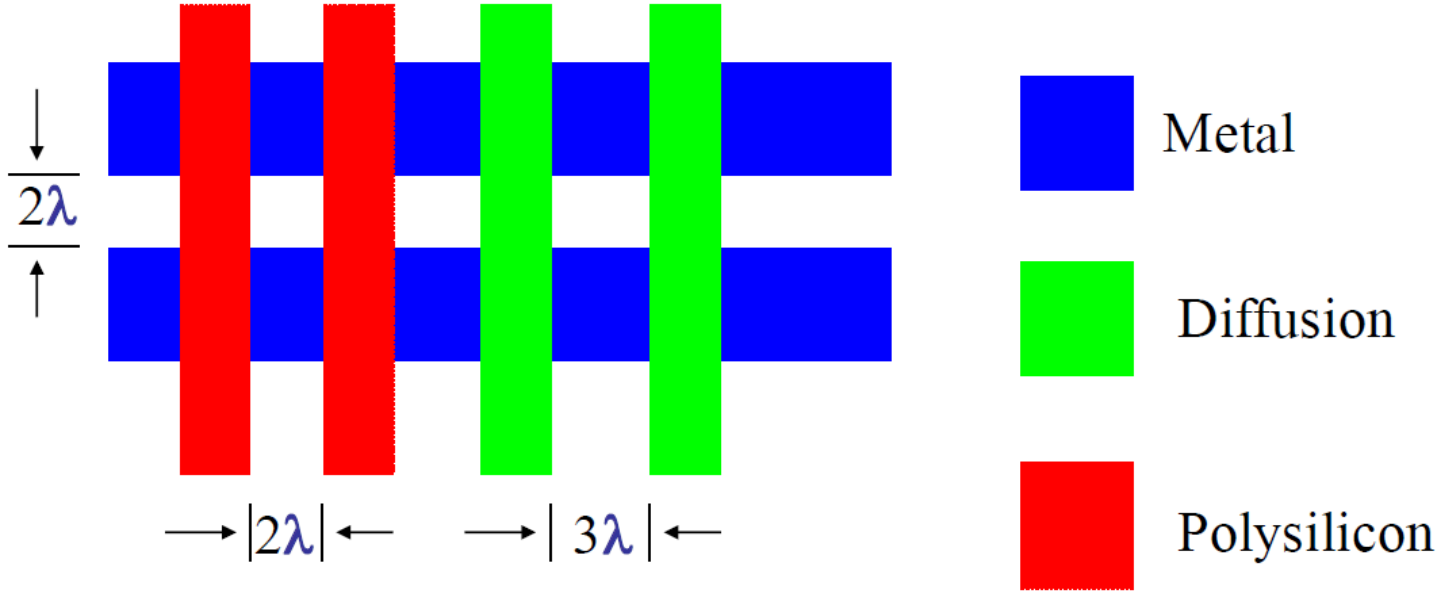
DESIGN RULES

- Minimum width of PolySi and diffusion line 2λ
- Minimum width of Metal line 3λ as metal lines run over a more uneven surface than other conducting layers to ensure their continuity



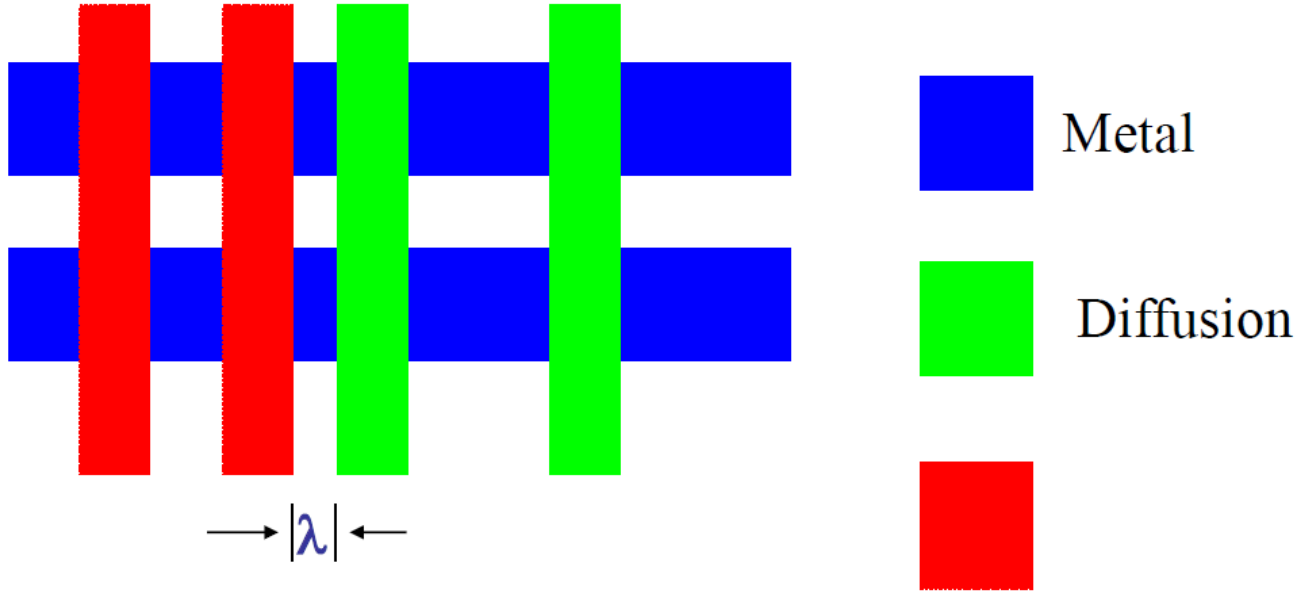
DESIGN RULES

- PolySi – PolySi space 2λ
- Metal - Metal space 2λ
- Diffusion – Diffusion space 3λ To avoid the possibility of their associated regions overlapping and conducting current



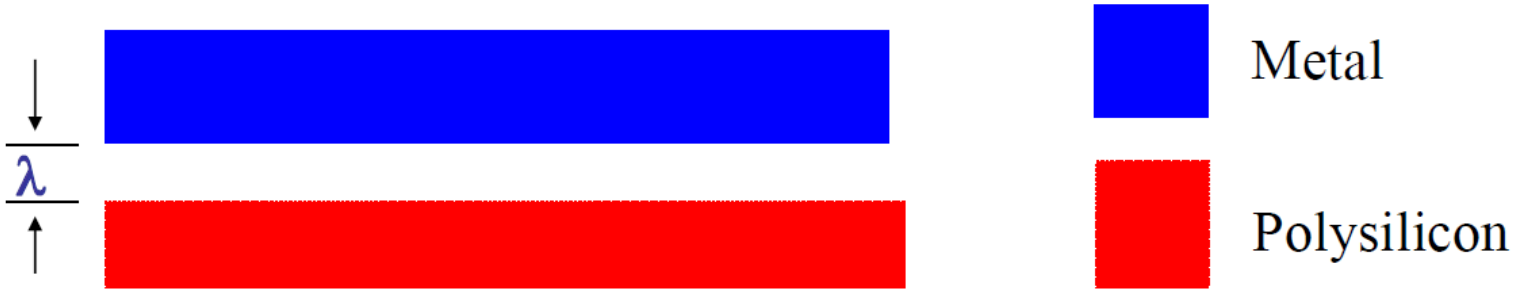
DESIGN RULES

- **Diffusion – PolySi space λ To prevent the lines overlapping to form unwanted capacitor**
- **Metal lines can pass over both diffusion and polySi without electrical effect. Where no separation is specified, metal lines can overlap or cross**



DESIGN RULES

- **Metal lines can pass over both diffusion and polySi without electrical effect**
- **It is recommended practice to leave λ between a metal edge and a polySi or diffusion line to which it is not electrically connected**



DESIGN RULES

- **Recall**
  - poly-poly spacing 2λ
  - diff-diff spacing 3λ (depletion regions tend to spread outward)
  - metal-metal spacing 2λ
  - diff-poly spacing λ