Phase Locked Loop (PLL)

The phase-locked loop (PLL) is an important building block of linear systems. Electronic phase- locked loop (PLL) came into vogue in the 1930 when it was used for radar synchronization and communication applications. Now with the advanced IC technology, PLLs are available as inexpensive monolithic lCs. **This technique for electronic frequency control is** used today in satellite communication systems, air borne navigational systems, FM communication systems, computers etc. The basic principle of PLL, different lCs and important applications are discussed.

Basic Principles

The basic block schematic of the PLL is shown in Fig. 4.1.1. This feedback system consists of Phase detector/comparator, low pass filter, error amplifier and Voltage Controlled Oscillator (VCO).

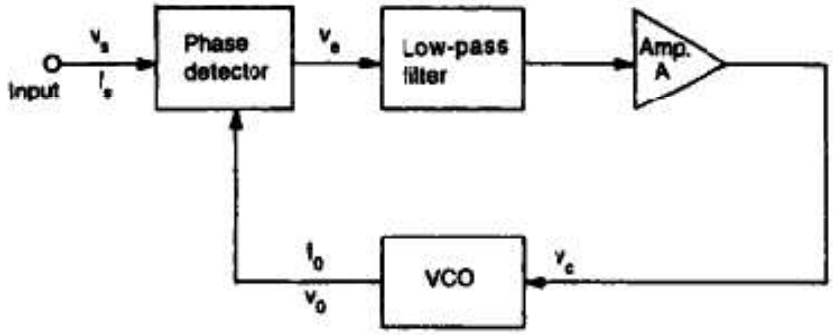


Fig. 1.Block schematic of the PLL

The phase detectors or comparator compares the input frequency f_{IN} with the feedback frequency $f_{OUT.}$ If the two signals differ in frequency and /or phase, a voltage ve is generated often referred to as the error voltage The output of the phase is then applied to the low-pass filter, which removes the high-frequency noise and produces a dc level. This dc level, in turn, is the input to the voltage-controlled oscillator (VCO). The output frequency of the VCO is directly proportional to the input dc level. The VCO frequency is compared with the input frequencies and adjusted until it is equal to the input frequencies.

Before the input is applied, the phase-locked loop is in the free-running state. Once the input frequency is applied, the VCO frequency starts to change and the phase-locked loop is said to be in the capture mode. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency fo of VCO is identical to fs except for a finite phase difference ϕ. This phase difference ϕ generates a corrective control voltage vc to shift the VCO frequency from fo to fs and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal through its repetitive action. Thus, a PLL goes through three stages (i) free running (ii) capture and (iii) locked or tracking.

(a) Phase detector:

The phase detector compares the input frequency and the VCO frequency and generates a dc voltage that is proportional to the phase difference between the two frequencies. Depending on the analoge or digital phase detector used, the PLL is either called an analog or digital type, respectively. Even though most of the monolithic PLL integrated circuits use analog phase detectors, the majority of discrete phase detectors in use are of the digital type mainly because of its simplicity

(b) Low-pass filter.

The second block shown in the PLL block diagram of Figure is a low-pass filter. The function of the low-pass filter is to remove the high-frequency components in the output of the phase detector and to remove high-frequency noise. More important, the 1ow-pass filter controls the dynamic characteristics of the phase locked loop. These characteristics include capture and lock ranges, bandwidth, and transient response. The capture range is always smaller than the lock range.

(c) Voltage-controlled oscillator:

A third section of the PLL is the voltage-controlled oscillator.The VCO is a free running multivibrator and operates at a set frequency fo called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage v_c to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a "Voltage Controlled Oscillator" or, in short, VCO.

The block diagram of the VCO is shown in Fig 4.12. The frequency of oscillations is determined by thee external R_1 and capacitor C_1 and the voltage V_C applied to the control terminal 5. The triangular wave is generated by alternatively charging the external capacitor C_1 by one current source and then linearly discharging it by another. The charging and discharging levels are determined by Schmitt trigger action. The Schmitt trigger also provides square wave output. Both the wave forms are buffered so that the output impedance of each is 50 ohms. Fig 4.12 (c) is a typical connection diagram. In this arrangement the R_1C_1 combination determines the free running frequency and the control voltage V_C at pin 5 is set by voltage divider formed with R_2 and R_3. The initial voltage V_C at pin 5 must be in the range

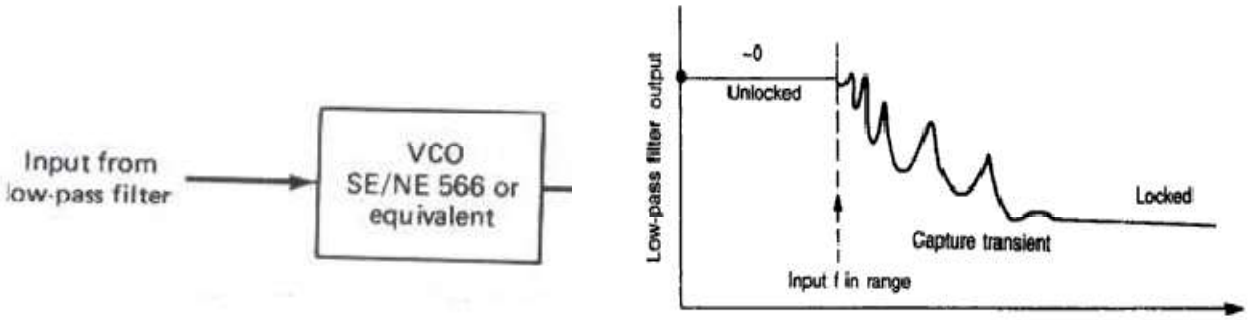
$$\frac{3}{4}(+V) \leq V_C \leq +V$$

Where +V is the total supply voltage. The modulating signal is ac coupled with the capacitor C

and must be <3 V_{PP}. The frequency of the output wave forms is approximated by

$$f_o \cong \frac{2(+V - V_C)}{R_1 C_1 (+V)}$$

Where R1should be in the range 2KΩ < R1< 20KΩ. For affixed VC and constant C1, the frequency f_O can be varied over a 10:1 frequency range by the choice of R1 between 2KΩ < R1< 20KΩ.



to the difference frequency between the VCO and the input signal. The dc component of the beat drives the VCO towards the lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency. The difference in frequency becomes smaller and a large de component is passed by the filter, shifting the VCO frequency further. The process continues until the VCO locks on to the signal and the difference frequency is dc.

The low pass filter controls the capture range. If VCO frequency is far away, the beat frequency will be too high to pass through the filter and the PLL will not respond. We say that the signal is out of the capture band. However, once locked, the filter no longer restricts the PLL. The VCO can track the signal well beyond the capture band. Thus tracking range is always larger than the capture range.

Lock-in Range

Once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. The lock range is usually expressed as a percentage of fo, the VCO frequency.

Capture Range

The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of fo.

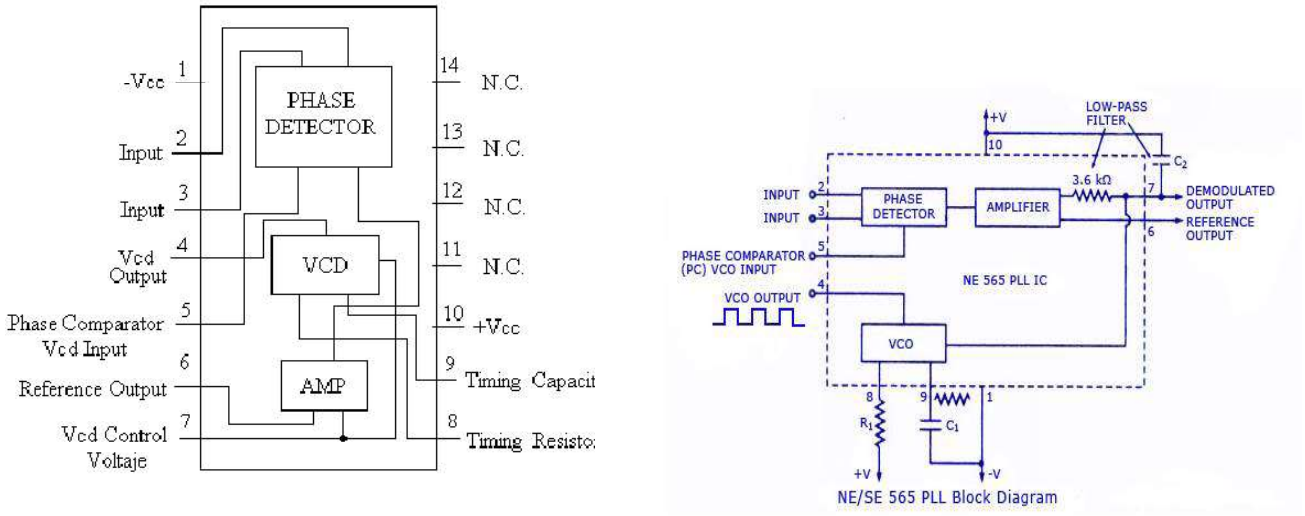
Pull-in. time

The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

Phase Locked Loop IC 565

IC565 is available as a 14 pin DIP package and as 10 pin metal can package. The pin configuration and the block diagram are shown in Fig.4.2.1 (a, b). The output frequency of the VCO (both inputs 2, 3 grounded) is given by

$$f_o = \frac{0.25}{R_T C_T} \text{ Hz}$$



Pin & block diagram NE/SE565 PLL

Where RT and CT are the external resistor and capacitor connected to pin 8 and pin 9. A value between 2 KΩ and 20KΩ is recommended for RT. The VCO free running frequency is adjusted with RT and CT to be at the centre of the input frequency range. It may be seen that phase locked loop is internally broken between the VCO output and phase comparator input. A short circuit between pins 4 and 5 connects the VCO output to the phase comparator so as to compare fo with input signal fs. A capacitor C is connected between pin 7 and pin 10 (supply terminal) to make a low pass filter with the internal resistance of 3.6 KΩ.

The important electrical parameters of 565 PLL are:

Operating frequency range	0.001 Hz to 500 KHz
Operating voltage range	±6V to ±12V
Input level	10 mV rms min. to 3V pp max.
Input impedance	10 KΩ
Triangle wave amplitude	2.4Vpp at ±6V supply voltage
Square wave amplitude	5.4Vpp at ±6V supply voltage