## 19.7 THE MOS DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD

We know that if the drain resistance $R_D$ of MOSFET amplifier is replaced by a constant current source, then this results in much higher voltage gain. The same idea applies to differential amplifier. The aim of this article is to consider the active loaded differential amplifier and converting the output from differential to a single ended. *The term active load refers to the use of current source in place of resistor as a load in the amplifier configuration.*

### 19.7.1 DIFFERENTIAL-TO-SINGLE-ENDED CONVERSION

We have considered the differential amplifier in which the output was taken between two drains (or collectors). This result in the double value of differential gain. Now, we consider the basic approach for differential to single-ended conversion in which the output is taken between the drain (or collector) of one transistor and ground. This is known as differential-to-single-ended conversion.

Figure (19·37) shows the simplest basic approach for differential-to-single ended conversion.

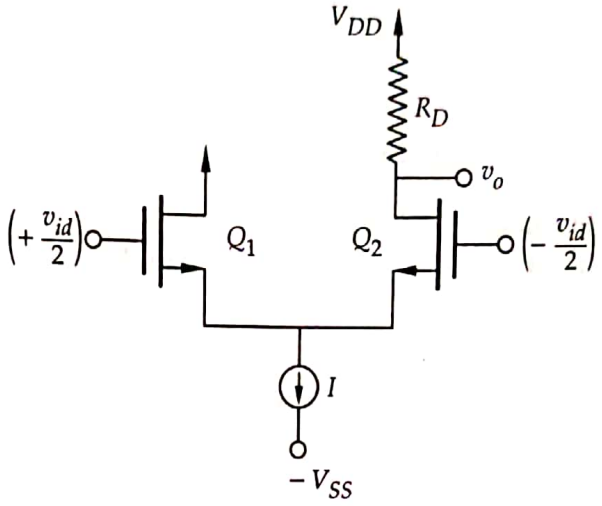



**Fig. 19·37** Simple approach for differential to single-ended conversion

In the circuit we ignore the drain current signal of transistor $Q_1$ and eliminate its drain resistor. The output is taken between drain of transistor $Q_2$ and ground. In such a situation, the grain reduces to half. Therefore, the drain current of $Q_1$ may be utilized in some other applications.

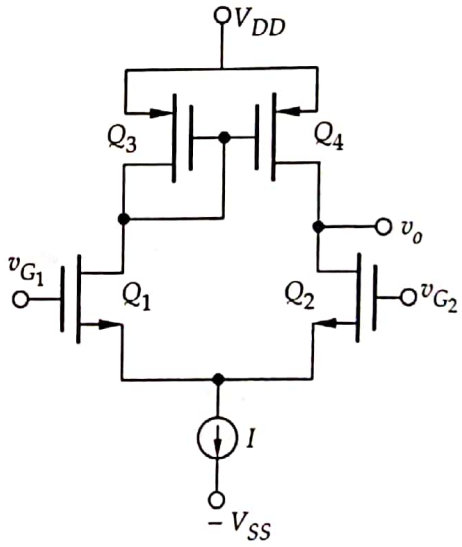



**Fig. 19·38** Active loaded MOS differential pair

#### 19.7-2 THE ACTIVE-LOADED MOS DIFFERENTIAL PAIR

We can use an active load in conjunction with MOSFET differential pair. Figure (19·38) shows a MOSFET differential amplifier formed by transistor $Q_1$ and $Q_2$ with an active load formed by transistors $Q_3$ and $Q_4$. These are known as current mirrors.

**When common-mode input signal is applied.**

To consider the operation of the circuit, let the two input terminals are connected to a d.c. voltage. In this case the output voltage will be zero. Let us consider the situation shown in fig. (19·39). We assume that the circuit is in perfect matching. The bias current $I$ is equally divided between $Q_1$ and $Q_2$. Now the

drain current $\left(\frac{I}{2}\right)$ of $Q_1$ is fed to the input of transistor of mirror $Q_3$. Further, a replica of this current is provided by the output transistor of the mirror $Q_4$. The drain voltage of $Q_4$ will track the voltage at the drain of $Q_3$. Therefore, the voltage at the output will be $V_{DD} - V_{SG_3}$.

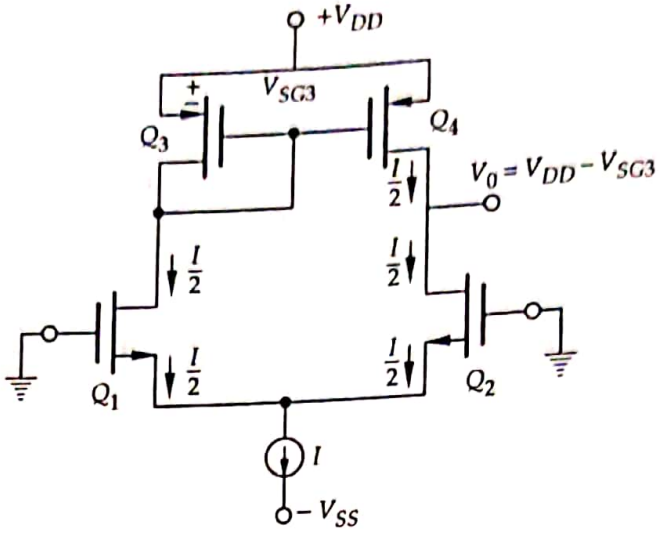



**Fig. 19·39** Circuit at equilibrium

**When differential-mode input signal is applied**

Next, we consider the circuit with a differential input signal $v_{id}$ applied to the input as shown in fig. (19·40).

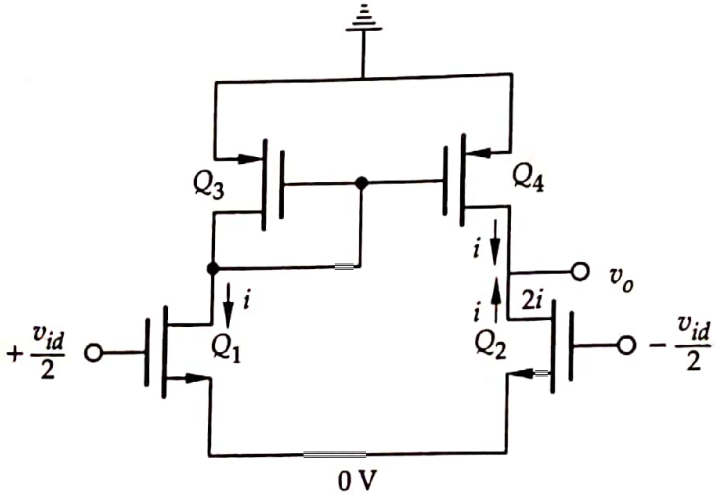



**Fig. 19·40** Circuit with differential input signal applied

When small signal input is applied, then in the equivalent circuit all the d.c. sources including $I$ are removed. We also ignore $r_0$ of all the transistors. It is obvious from the fig. (19·40) that a virtual ground will develop at common-source terminal of $Q_1$ and $Q_2$. Transistor $Q_1$ conducts a current $i = g_{m_1}(v_{id}/2)$ and $Q_2$ also conducts an equal current but in opposite direction. The drain signal current of $Q_1$ is fed to the input of $Q_3 - Q_4$ mirror. As a result, the transistor $Q_4$ provided a drain current $i$. Now, the output current is $2i$. The factor 2 is a result of current mirror action. If a load resistance is connected to the output node, the current $2i$ will flow through it giving an output voltage $v_0$. In the absence of the output load, the output voltage will be determined by the output current $2i$ and output resistance of the circuit.

### 19.7-3 DIFFERENTIAL GAIN OF THE ACTIVE-LOADED MOS PAIR ($A_d$)

The aim of this article is to derive an expression for the differential gain ($v_0/v_{id}$) of active loaded MOS differential pair. We shall also take into consideration the input resistance $r_0$ of the transistor.

Figure (19·41) shows a MOSFET differential amplifier with active load. $Q_1$ and $Q_2$ are $n$-channel devices and form the differential pair. The differential pair is biased with a current source $I$. The load circuit consists of transistors $Q_3$ and $Q_4$ both $p$-channel devices and connected in current mirror configuration. A one sided output is taken from the common drains of $Q_2$ and $Q_4$.

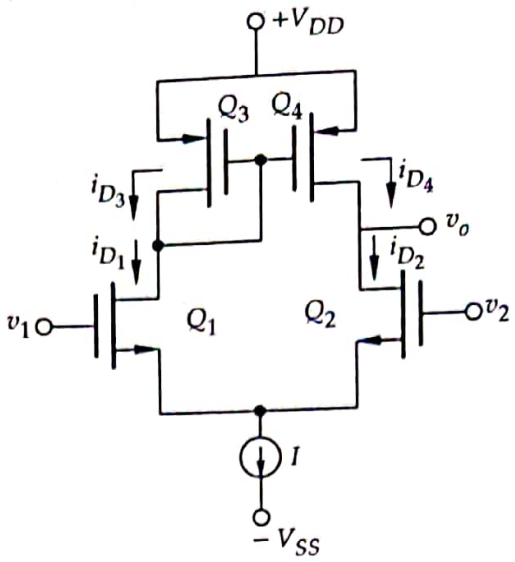



**Fig. 19·41** MOSFET differential amplifier with active load

When a common-mode voltage of $v_1 = v_2 = v_{CM}$ is applied, the current $I$ splits evenly between $Q_1$ and $Q_2$. In this case, $I_{D_1} = I_{D_2} = I/2$. Further, there are no gate currents, *i.e.* $i_{D_3} = i_{D_1}$ and $i_{D_4} = i_{D_2}$.

If a small differential mode input voltage $v_{id} = v_1 - v_2$ is applied then the drain currents $i_{D_1}$ and $i_{D_2}$ of transistors $Q_1$ and $Q_2$ are expressed as

$$i_{D_1} = \frac{I}{2} + i_d \qquad \ldots(1)$$

and

$$i_{D_2} = \frac{I}{2} - i_d \qquad \ldots(2)$$

where $i_d$ is signal current.

For small value of $v_{id}$, we have

$$i_d = \frac{(g_m v_{id})}{2} \qquad \ldots(3)$$

It is obvious from the fig. (19·41) that $M_1$ and $M_3$ are in series, therefore,

$$i_{D_3} = i_{D_1} = \frac{I}{2} + i_d \qquad \ldots(4)$$

As $M_3$ and $M_4$ constitute the current mirrors and hence,

$$i_{D_4} = i_{D_3} = \frac{I}{2} + i_d \qquad \ldots(5)$$

Figure (19·42) shows the equivalent circuit of differential amp. with active load and showing the signal currents.

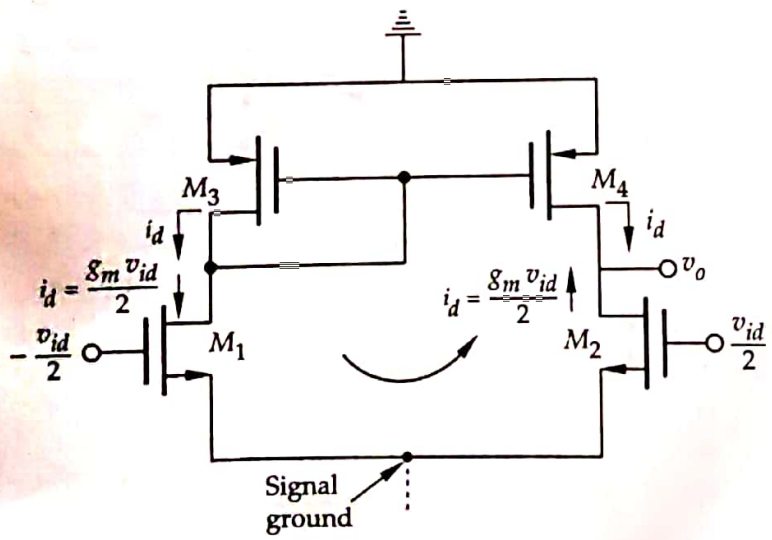
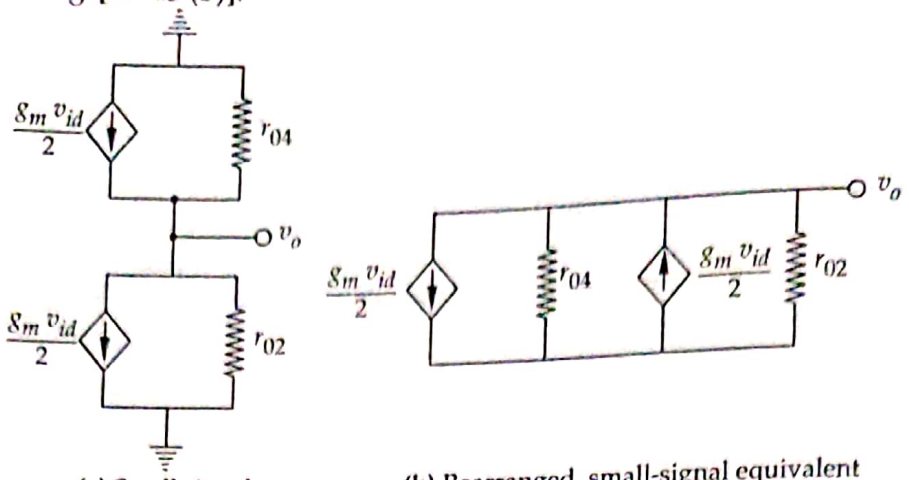



**Fig. 19·42** Equivalent circuit of MOSFET differential amplifier with active load

Figure [19·43 (a)] shows the a.c. equivalent circuit of diff. amp. with active load at the drain node of $M_2$ and $M_4$. The circuit is rearranged by combining the signal grounds at a common point as shown in fig. [19·43 (b)].




(a) Small signal equivalent circuit

(b) Rearranged small-signal equivalent circuit

**Fig. 19·43**

From fig. [19·43 (b)] $$v_0 = 2\left(\frac{g_m v_{id}}{2}\right)(r_{02} \| r_{04}) \quad \ldots(6)$$

Therefore, small signal differential-mode voltage gain is

$$A_d = \frac{v_0}{v_{id}} = g_m (r_{02} \| r_{04}) \quad \ldots(7)$$

In case $r_{02} = r_{04} = r_0$, then

$$\boxed{A_d = \frac{1}{2} g_m r_0 = \frac{A_0}{2}} \quad \ldots(8)$$

where $A_0$ is the intrinsic gain of MOS transistor.

### 19.7-4 OUTPUT RESISTANCE $R_0$

Figure (19·44) shows the circuit for determining the output resistance $R_0$. The current distribution is also shown in the figure.

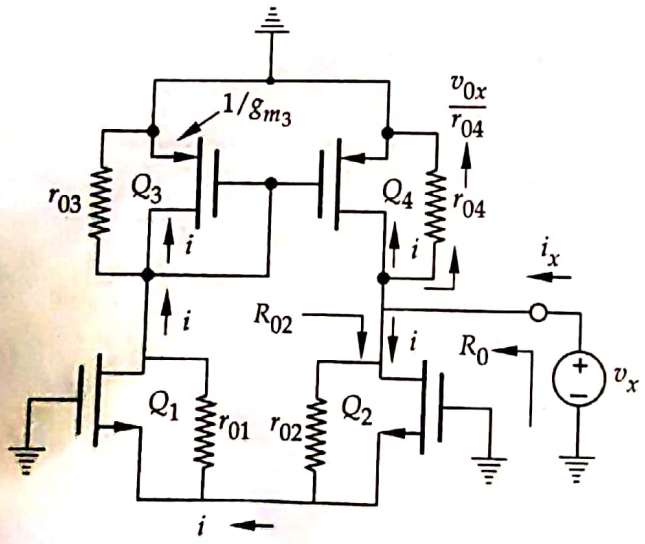



**Fig. 19·44** Circuit for determining $R_0$

The transistor $Q_2$ is a common gate transistor. Its source lead is connected to the input resistance of transistor $Q_1$. The latter is connected in common gate configuration with a small resistance in the drain. This is approximately equal to $\frac{1}{g_{m3}}$. Therefore, the input resistance is approximately $\frac{1}{g_{m1}}$. Now, the output resistance of transistor $Q_2$ is

$$R_{02} = r_{02} + (1 + g_{m2}\, r_{02}) \left(\frac{1}{g_{m1}}\right)$$

or $$R_{02} = 2\, r_{02} \qquad (\because g_{m2}\, r_{02} >> 1 \text{ and } g_{m1} = g_{m2} = g_m) \qquad \ldots(9)$$

At the output, node,

$$i_x = i + i + \left(\frac{v_x}{r_{04}}\right) = \left(2i + \frac{v_x}{r_{04}}\right) \qquad \ldots(10)$$

or $$i_x = 2\left(\frac{v_x}{R_{02}}\right) = \left(\frac{v_x}{r_{04}}\right)$$

or $$i_x = 2\left(\frac{v_x}{2r_{02}}\right) + \left(\frac{v_x}{r_{04}}\right) = \left(\frac{v_x}{r_{02}} + \frac{v_x}{r_{04}}\right)$$

or $$i_x = v_x \left[\frac{1}{r_{02}} + \frac{1}{r_{04}}\right] = v_x \left(\frac{r_{04} + r_{02}}{r_{02}\, r_{04}}\right)$$

The output resistance $R_0$ is given by

$$R_0 = \frac{v_x}{i_x} = (r_{02} \,\|\, r_{04})$$

Therefore, $$\boxed{R_0 = (r_{02} \,\|\, r_{04})} \qquad \ldots(11)$$

The differential gain is given by $A_d = \frac{v_0}{i_d} = g_m R_0$

$$\boxed{A_d = g_m\, (r_{02} \,\|\, r_{04})} \qquad \ldots(12)$$

### 19.7-5 DETERMINATION OF TRANSCONDUCTANCE ($G_m$)

Figure (19·45) shows the circuit arrangement for determining $G_m$. In the circuit, the output current is short circuited to ground to find $G_m$. Now, the circuit becomes symmetrical because the voltage between drain of $Q_1$ and ground is very small. This is due to low resistance between that node and ground which is equal to $1/g_{m3}$. The simplified equivalent circuit of each pair is shown in fig. [19·46 (a) and (b)].

From fig. [19·46 (a)], the voltage $v_{gs3}$ is given by

$$v_{gs3} = -g_{m1} \left(\frac{1}{g_{m3}} \,\|\, r_{03} \,\|\, r_{01}\right) \qquad \ldots(13)$$

As $r_{01}$ and $r_{03} >> (1/g_{m3})$, eq. (13) can be written as

$$v_{gs3} \cong -g_{m1} \left(\frac{v_{id}}{2}\right)\left(\frac{1}{g_{m3}}\right) \cong -\left(\frac{g_{m1}}{g_{m3}}\right)\left(\frac{v_{id}}{2}\right) \qquad \ldots(14)$$

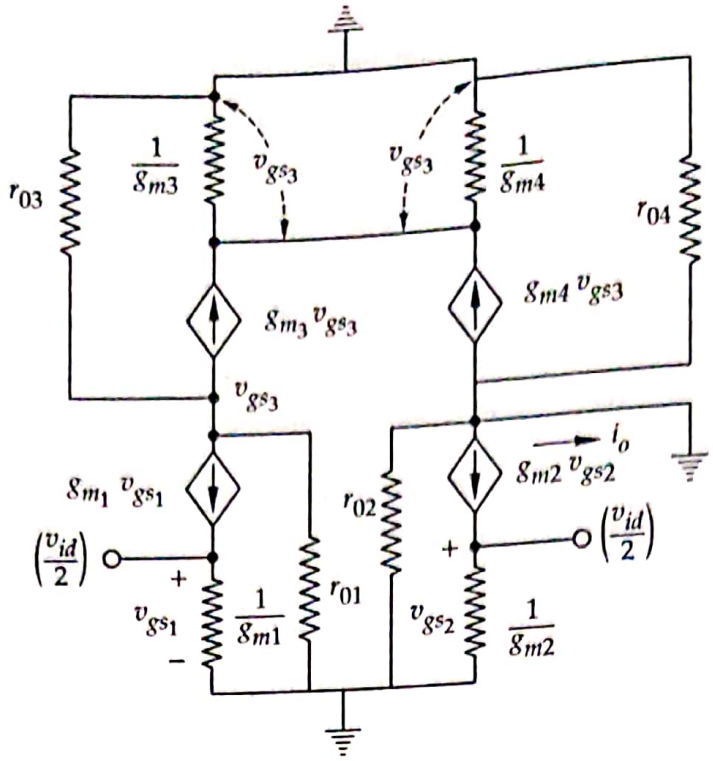



**Fig. 19·45**

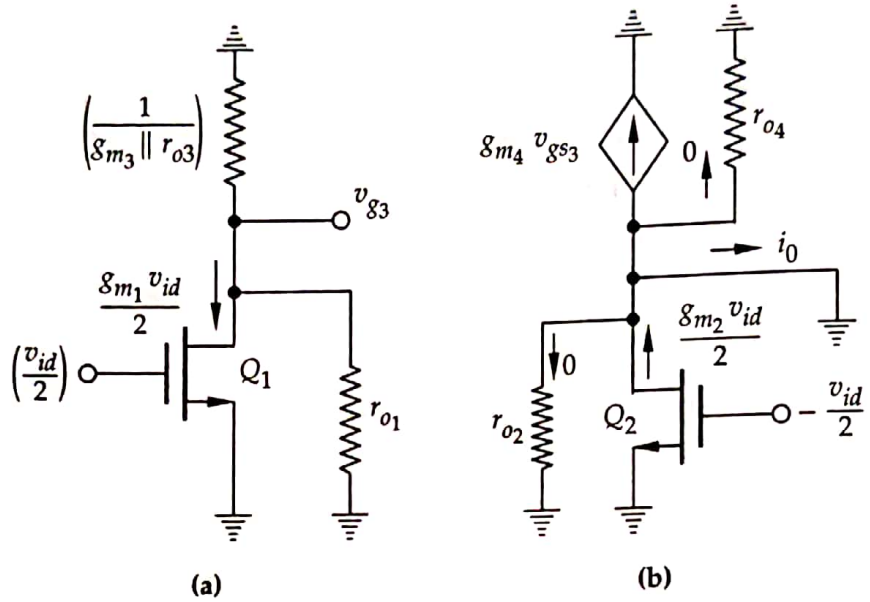



**Fig. 19·46** Determination of transconductance $G_m$

This voltage controls the grain current of $Q_4$ resulting in a current $g_{m4}\ v_{gs3}$.
The output current $i_0$ is given by

$$i_0 = -g_{m4}\ v_{gs3} + g_{m2}\left(\frac{v_{id}}{2}\right) \qquad \ldots(15)$$

**It is important to mention here that ground at the output node causes the currents $r_{02}$ and $r_{04}$ to be zero as shown in fig. [19·46 (b)].**

**Substituting the value of $v_{gs3}$ from eq. (14) in eq. (15) we get**

$$i_0 = g_{m4}\left(\frac{g_{m1}}{g_{m3}}\right)\left(\frac{v_{id}}{2}\right) + g_{m2}\left(\frac{v_{id}}{2}\right) \qquad \ldots(16)$$

**If $g_{m3} = g_{m4}$ and $g_{m_1} = g_{m2} = g_m$, then**

$$i_0 = g_m \left(\frac{v_{id}}{2}\right) + g_m \left(\frac{v_{id}}{2}\right) \quad \ldots(17)$$

or $$i_0 = g_m\, v_{id}$$

Now $$\boxed{G_m = \left(\frac{i_0}{v_{id}}\right) = g_m} \quad \ldots(18)$$

### 19.7-6 COMMON-MODE GAIN ($A_{CM}$)

The common mode MOS differential amplifier has a low gain but it has a high CMRR. Figure (19·47) shows the circuit with $v_{iCM}$ applied and eliminating the power supplies. We have included the output resistance $R_{SS}$ of bias current source. To make the circuit symmetrical, the contribution of $R_{SS}$ is divided in the source of $Q_1$ and $Q_2$ as $2\,R_{SS}$. $2\,R_{SS}$ is usually much larger than $(1/g_m)$ of each of transistors $Q_1$ and $Q_2$, and hence, the signals at the source terminals will be approximately equal to $v_{iCM}$. The effect of $r_{01}$ and $r_{02}$ is also negligibly small.

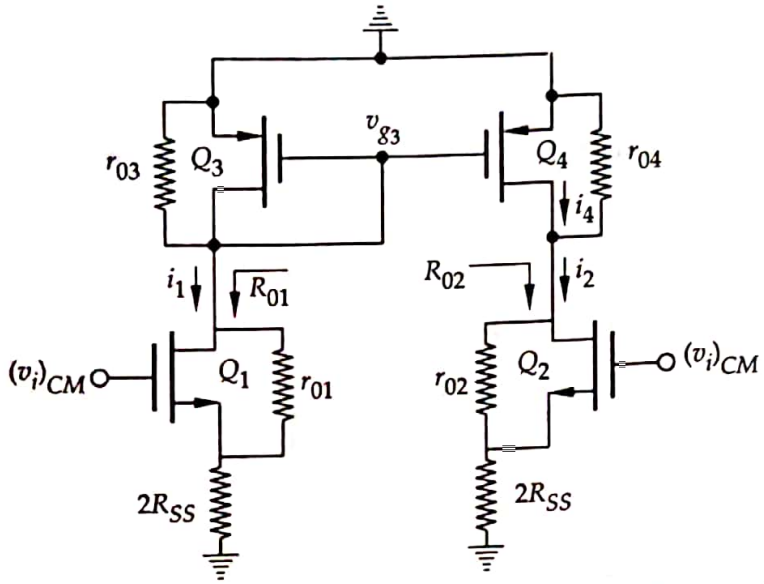
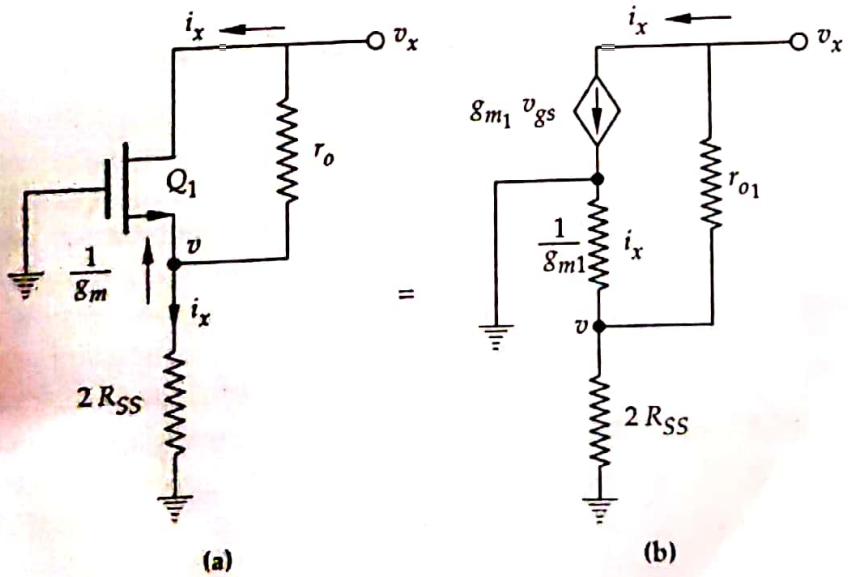



**Fig. 19·47** Analysis of the active loaded MOS differential amplifier

The current $i_1$ and $i_2$ of transistors $Q_1$ and $Q_2$ respectively can be written as

We have, $$i_1 = i_2 = \frac{(v_i)_{CM}}{2\,R_{SS}} \quad \ldots(19)$$

The output resistance of each transistor can be obtained by using fig. (19·48).




(a) (b)

**Fig. 19·48**

The voltage at node $v$ is given by

$$v = i_x \ (2 R_{SS}) = 2 i_x \ R_{SS}$$

Using circuit [19·48 (b)], we have

$$\begin{aligned} v_x &= i_x r_{01} + g_{m1} v + v \\ &= i_x r_{01} + 2 g_{m1} i_x R_{SS} r_{01} + 2 i_x R_{SS} \\ &= i_x [r_{01} + 2 g_{m_1} R_{SS} r_{01} + 2 R_{SS}] \end{aligned}$$

Therefore, $$R_{01} = r_{01} + 2 g_{m_1} R_{SS} r_{01} + 2 R_{SS} \quad \ldots(20)$$

or $$R_{01} = R_{02} = r_0 + 2 R_{SS} + 2 g_m r_0 R_{SS}$$

where $r_{01} = r_{02} = r_0$ and $g_{m1} = g_{m2} = g_m$. We can neglect $R_{01}$ and $R_{02}$ in finding the total resistance between each of the drain nodes and ground.

The current $i_1$ is pased through $[(1 / g_{m3}) \| r_{03}]$. This produces a voltage $v_{g3}$ given by

$$v_{g3} = -i_1 \left( \frac{1}{g_{m3}} \| \ r_{03} \right) \quad \ldots(21)$$

Resistor $r_{04}$ senses this voltage and hence, provides a drain current $i_4$

$$i_4 = -g_{m4} \ v_{g3} = g_{m4} \ i_1 \left( \frac{1}{g_{m3}} \| \, r_{03} \right) \quad \ldots(22)$$

Now, $$v_0 = (i_4 - i_2) \, r_{04}$$

or $$v_0 = \left[ g_{m4} \ i_1 \left( \frac{1}{g_{m3}} \| \, r_{03} \right) - i_2 \right] r_{04} \quad \ldots(23)$$

or $$v_0 = i_1 \left[ g_{m4} \left( \frac{1}{g_{m3}} \| \, r_{03} \right) - 1 \right] r_{04} \qquad (\because \ i_1 = i_2)$$

$$= \frac{v_{iCM}}{2 R_{SS}} \left[ g_{m4} \left( \frac{1}{g_{m3}} \| \, r_{03} \right) - 1 \right] r_{04}$$

$$= \frac{v_{iCM}}{2 R_{SS}} \left[ g_{m4} \left( \frac{r_{03}}{g_{m3} \ r_{03} + 1} \right) - 1 \right] r_{04}$$

$$= \frac{v_{iCM}}{2 R_{SS}} \left[ \frac{g_{m4} \ r_{03} - g_{m3} \ r_{03} - 1}{g_{m3} \ r_{03} + 1} \right] r_{04}$$

$$= \frac{v_{iCM}}{2 R_{SS}} \left[ \frac{-1}{g_{m3} \ r_{03} + 1} \right] r_{04} \qquad (\because g_{m3} = g_{m4})$$

$\therefore$ $$v_0 = -\frac{v_{iCM} \, r_{04}}{2 R_{SS} (1 + g_{m3} \ r_{03})} \quad \ldots(24)$$

**Usually $g_{m3} \ r_{03} >> 1$ and $r_{03} = r_{04}$. Therefore,**

$$v_0 = i \frac{v_{iCM}}{2 R_{SS} \, g_{m3}}$$

Therefore,
$$A_{CM} = \frac{v_0}{v_{iCM}} = -\frac{1}{2\, g_{m3}\, R_{SS}} \quad \ldots(25)$$

## 19.7-7 COMMON MODE REJECTION RATIO (CMRR)

$$\text{CMRR} = \frac{|A_d|}{|A_{CM}|} = \frac{[g_m\,(r_{o1} \,||\, r_{o4})]}{(1/2\, g_{m3}\, R_{SS})}$$

or
$$\text{CMRR} = g_m\,(r_{o2} \,||\, r_{o4}) \times (2\, g_{m3}\, R_{SS}) \quad \ldots(26)$$

For $r_{02} = r_{04} = r_0$ and $g_{m3} = g_m$, we get

$$\text{CMRR} = g_m \left(\frac{r_o}{2}\right) \times 2\, g_m\, R_{SS}$$

or
$$\text{CMRR} = (g_m\, r_o)\,(g_m\, R_{SS}) = g_m^{\,2}\, r_o\, R_{SS} \quad \ldots(27)$$