SOLVED EXAMPLES

Example 1 *A MOS differential pair with common-mode voltage is shown in fig. (19·54). In the figure,* $V_{DD} = V_{SS} = 1{\cdot}5$ V, $K_n'(W/L) = 4$ mA / V^2, $V_t = 0{\cdot}5$ V, $I = 0{\cdot}4$ mA *and* $R_D = 2{\cdot}5$ kΩ.

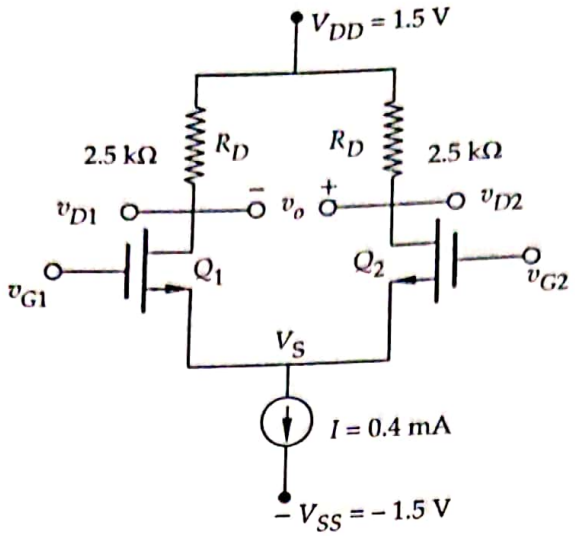

Fig. 19·54 MOS differential pair with common-mode

Find the following:

(a) Find V_{oV} and V_{GS} for each transistor.

(b) For $v_{CM} = 0$, find v_S, i_{D1}, v_{D1} and v_{D2}.

(c) Repeat (b) for $v_{CM} = 1$ V.

(d) What is the highest value of v_{CM} for which the transistors Q_1 and Q_2 remain in saturation?

(e) If current source I requires a minimum voltage of 0·4 V to operate properly, what is the lowest value allowed for v_S and hence for v_{CM}?

(a) The over drive voltage is given by

$$V_{0V} = \left[\frac{I}{k_n'(W/L)}\right]^{1/2} \qquad \text{[Eq. (7) of article 19.1-1]}$$

$$= \left[\frac{0{\cdot}4 \times 10^{-3}}{4 \times 10^{-3}}\right]^{1/2} = \mathbf{0{\cdot}32\ V}$$

Now $V_{GS} = V_{0V} + V_t = 0{\cdot}32 + 0{\cdot}5 = \mathbf{0{\cdot}82\ V}$

(b) $v_{CM} = 0$ V

In this case, $I = 0{\cdot}4$ mA or $I/2 = 0{\cdot}2$ mA

$$V_S = -v_{GS} = \mathbf{-0{\cdot}82\ V}$$

$$\therefore \quad i_{D_1} = i_{D_2} = \frac{I}{2} = \mathbf{0{\cdot}2\ mA}$$

and, $v_{D_1} = V_{DD} - i_{D_1} R_D = 1{\cdot}5 - [(0{\cdot}2 \times 10^{-3}) \times (2{\cdot}5 \times 10^{3})] = \mathbf{1\ V}$

$V_{D_2} = \mathbf{1\ V}$

(c) Figure (19·55) shows the differential amplifier with common-mode input voltage $v_{CM} = 1$ V.

$$v_S = v_{CM} - v_{GS} = 1 - 0{\cdot}82 = \mathbf{+0{\cdot}18\ V}$$

Scanned with CamScanner

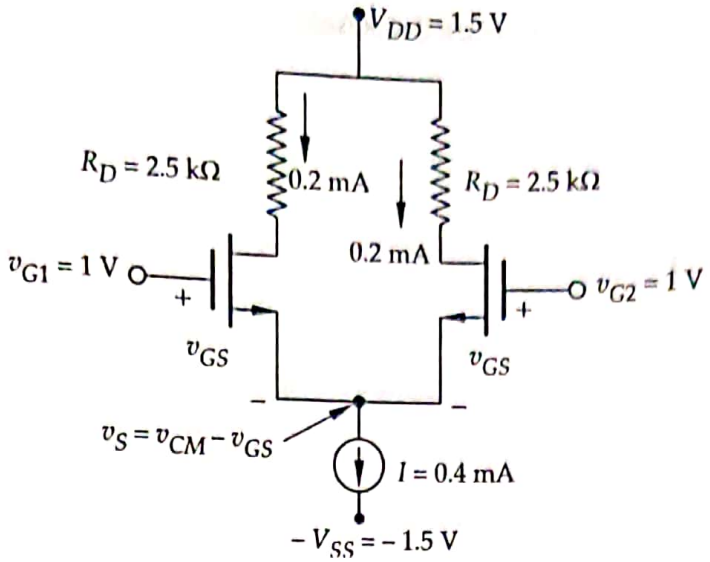

Fig. 19·55 Differential amplifier with common-mode input voltage 1 V

$$i_{D_1} = i_{D_2} = \frac{I}{2} = 0{\cdot}2 \text{ mA}$$

$$v_{D_1} = v_{D_2} = V_{DD} - i_D R_D = 1{\cdot}5 - [(0{\cdot}2 \times 10^{-3}) \times (2{\cdot}5 \times 10^3)]$$

$$= 1{\cdot}5 - 0{\cdot}5 = \mathbf{1 \text{ V}}$$

(d) $(v_{CM})_{max} = V_t + V_{DD} - (I/2) R_D$

$$= 0{\cdot}5 + 1{\cdot}5 - [(0{\cdot}2 \times 10^{-3}) \times (2{\cdot}5 \times 10^3)]$$

$$= 0{\cdot}5 + 1{\cdot}5 - 0{\cdot}5 = \mathbf{1{\cdot}5 \text{ V}}$$

(e) $(v_{CM})_{min} = -V_{SS} + V_S + V_t + V_{0V}$

$$= -1{\cdot}5 + 0{\cdot}4 + 0{\cdot}5 + 0{\cdot}32 = \mathbf{-0{\cdot}28 \text{ V}}$$

$$(v_S)_{min} = (v_{CM})_{min} - v_{GS} = -0{\cdot}28 - 0{\cdot}82 = \mathbf{-1{\cdot}1 \text{ V}}$$

Example 2 *A* PMOS *differential amplifier is shown in fig.* (19·56). *Here,* $V_{tp} = -0{\cdot}8$ V, *and* $K_p'(W/L) = 3{\cdot}5$ mA / V^2.

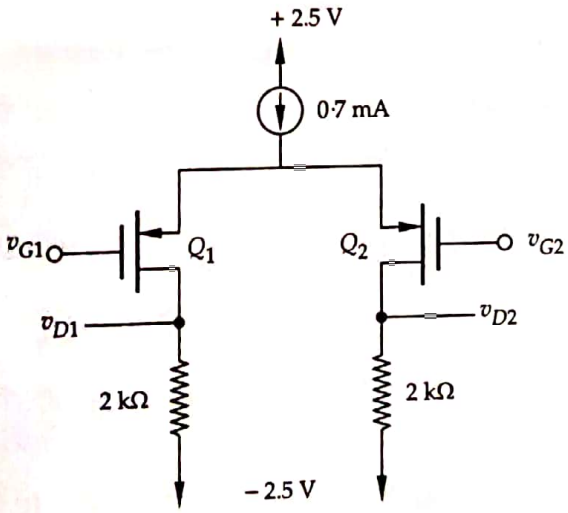

Fig. 19·56 PMOS differential amplifier

(a) Find V_{oV} *and* V_{GS} *for each transistor for* $v_{G1} = v_{G2} = 0$ V.

(b) Find v_S, V_{D1} *and* V_{D2} *for* $v_{G1} = v_{G2} = 0$ V.

Scanned with CamScanner

(c) If the current source requires a minimum voltage of 0·5 V, find the input common-mode range.

$$V_{DD} = V_{SS} = 2{\cdot}5\text{ V} \text{ and } K_p'(W/L) = 3{\cdot}5\text{ mA/V}^2$$

(a) Overdrive voltage V_{0V} is given by

$$V_{0V} = -\left[\frac{I}{K_p'(W/L)}\right]^{1/2} = -\left[\frac{0{\cdot}7\times10^{-3}}{(3{\cdot}5\times10^{-3})}\right]^{1/2} = \mathbf{-0{\cdot}45\text{ V}}$$

The gate-source voltage v_{GS} is given by

$$v_{GS} = V_{0V} - V_{tp} = -0{\cdot}45 - 0{\cdot}8 = \mathbf{-1{\cdot}25\text{ V}}$$

(b) Source voltage is given by

$$v_{S1} = v_{S2} = v_G - v_{GS} = 0 + 1{\cdot}25\text{ V} = \mathbf{1{\cdot}25\text{ V}}$$

Drain voltage is given by

$$v_{D1} = v_{D2} = \left(\frac{I}{2}\right)R_D - V_{DD} = \frac{0{\cdot}7}{2}\times 2 - 2{\cdot}50 = \mathbf{-1{\cdot}8\text{ V}}$$

(c) For Q_1 and Q_2 to remain in saturation

$$v_{DS} \le v_{GS} - v_{tp}$$

or $$v_{CM} \ge \left(\frac{I}{2}R_D - V_{DD}\right) + V_{tp}$$

or $$(v_{CM})_{\min} = \left(\frac{0{\cdot}7}{2}\times 2 - 2{\cdot}5\right) - 0{\cdot}8 = \mathbf{-2{\cdot}6\text{ V}}$$

To allow sufficient voltage for the current source to operate properly

$$v_{CM} \le V_{SS} - V_{CS} + (V_{tp} + V_{0V})$$

or $$(v_{CM})_{\max} = 2{\cdot}5 - 0{\cdot}5 - 1{\cdot}25 = \mathbf{0{\cdot}75\text{ V}}$$

Example 3 *A PMOS differential pair operated at a bias current of* 0·8 mA *employs transistors with* $(W/L) = 100$, $\mu_n C_{ox} = 0{\cdot}2\text{ mA/V}^2$, $R_D = 5\text{ k}\Omega$ *and* $R_{SS} = 25\text{ k}\Omega$.

(a) Find the differential gain, common-mode gain and common-mode rejection ratio (CMRR) *in* dB.
(b) Repeat (a) when the output is taken differentially.
(c) Repeat (a) when the output is taken differentially but the drain resistance have a 1% *mismatch.*

Let us first calculate value of g_m.

We know that, $i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\cdot V_{0V}^2$

$$\therefore \quad 0{\cdot}4\times10^{-3} = \frac{1}{2}(0{\cdot}2\times10^{-3})\,100\times V_{0V}^2 \qquad \left(\because i_D = \frac{I}{2} = 0{\cdot}4\text{ mA}\right)$$

or $$V_{0V} = 0{\cdot}2\text{ V}$$

Therefore, $$g_m = \frac{i_D}{V_{0V}} = \frac{0{\cdot}4\times10^{-3}}{0{\cdot}2} = 2\text{ mA/V}$$

(a) Differential gain, $A_d = \frac{1}{2}g_m R_D = \frac{1}{2}\times(2\times10^{-3})\times(5\times10^3) = 5$

Common-mode gain $A_{CM} = -\frac{R_D}{2R_{SS}} = -\frac{5\times10^3}{2\times(25\times10^{-3})} = \mathbf{-0{\cdot}1}$

Scanned with CamScanner

Common-mode rejection ratio CMRR $= \dfrac{5}{0{\cdot}1} = 50$

CMRR in dB $= 20 \log (50) = 34$ dB

(b) $A_d = g_m R_D = (2 \times 10^{-3}) \times (5 \times 10^3) = 10$

Common-mode gain $A_{CM} = 0$

CMRR in dB $= 20 \log \left(\dfrac{A_d}{A_{CM}} \right) = \infty$ dB

(c) Mismatch in R_D will have negligible effect on the differential gain

$\therefore \quad A_d \cong g_m R_D = (2 \times 10^{-3}) \times (5 \times 10^3) = 10$

Mismatch on R_D effect on common-mode gain

$$A_{CM} = -\frac{R_D}{2 R_{SS}} \left(\frac{\Delta R_D}{R_D} \right)$$

Given $\Delta R_D = 1\,\%$ of $R_D = 50\,\Omega$

$$A_{CM} = \frac{5000}{2 \times 25{,}000} \times \left(\frac{50}{5000} \right) = 0{\cdot}001$$

$$\text{CMRR in dB} = 20 \log \left(\frac{A_d}{A_{CM}} \right) = 20 \log \left(\frac{10}{0{\cdot}001} \right) = 80 \text{ dB}$$

Example 4. *Two identical silicon transistors with* $\beta = 50$, $V_{BE} = 0{\cdot}7$ V *at* $T = 25°C$, $V_{CC} = 20{\cdot}7$ V, $R_1 = 10$ kΩ *and* $R_C = 5$ kΩ *are used in the circuit shown in fig.* (19·57). *(i) Find the current* $I_{B_1}, I_{B_2}, I_{C_1}, I_{C_2}$ *at* 25°C, *(ii) Find* I_{C_2} *at* $T = 175°$ C *when* $\beta = 98$ *and* $V_{BE} = 0{\cdot}22$ V.

The current through resistor R_1 **[U.P.S.C., I.E.S. 2005]**

$$I = I_{C_1} + I_{B_1} + I_{B_2}$$

$$\cong I_C + 2 I_{B_1} = \beta I_{B_1} + 2 I_{B_1}$$

$$= (\beta + 2)\, I_{B_1} \quad \text{or} \quad I_{B_1} = \frac{I}{\beta + 2} \qquad \ldots(1)$$

Applying KVL to emitter loop of transistor Q_1, we have

$$V_{CC} = I R_1 - V_{BE} = 0 \qquad \ldots(2)$$

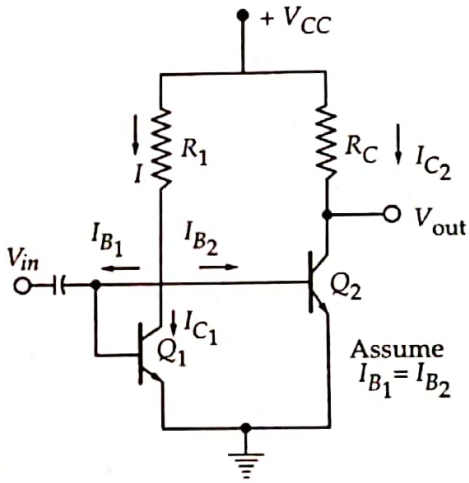

Fig. 19·57

(i) From eq. (2), we have

$$I = \frac{V_{CC} - V_{BE}}{R_1} = \frac{20{\cdot}7 - 0{\cdot}7}{10 \times 10^3} = 2 \text{ mA}$$

$$I_{B_1} = I_{B_2} = \frac{I}{\beta + 2} = \frac{2 \text{ mA}}{2 + 50} = 0{\cdot}0385 \text{ mA}$$

$$I_{C_1} = I_{C_2} = \beta I_{B_1} = 50 \times 0{\cdot}0385 \text{ mA} = 1{\cdot}92 \text{ mA}$$

(ii) At temperature $T = 175°C$

$$I_{C_2} = \beta I_{B_2} = \left(\frac{\beta}{\beta + 2} \right) I = \left(\frac{\beta}{\beta + 2} \right) \left(\frac{V_{CC} - V_{BE}}{R_1} \right)$$

or $$I_{C_2} = \left(\frac{98}{98 + 2} \right) \left(\frac{20{\cdot}7 - 0{\cdot}22}{10 \times 10^3} \right) = \left(\frac{98}{100} \right) \times \left(\frac{20{\cdot}48}{10 \times 10^3} \right) = 2 \text{ mA}$$

Scanned with CamScanner

Example 5. *In the circuit shown in* fig. (19·58), *the two transistors are matched. Find an expression for* I_1 *in terms of* I_{C_1} *and* β.

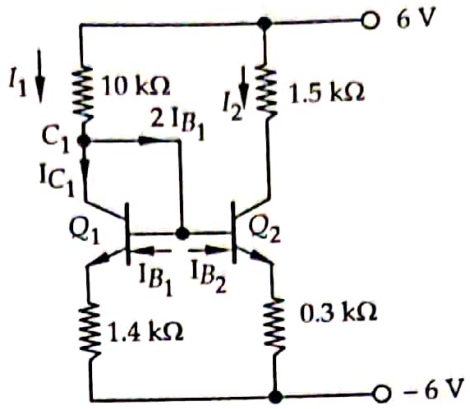

Fig. 19·58

Assume $V_{BE} = 0 \cdot 6$ V *and* β *to be large, calculate* I_1 *and* I_2. *Calculate* I_{C_1} *when* $\beta = 20$.

[U.P.S.C., I.E.S. 2007]

Here, the transistors are matched. Therefore, base current would be the same.

Applying KCL to collector terminal C of transistor Q_1, we have

$$I_1 = I_{C_1} + 2\, I_{B_1} = I_{C_1} + 2\, I_{C_1}/\beta = I_{C_1}\left(1 + \frac{2}{\beta}\right)$$

or $$I_1 = \left(\frac{\beta + 2}{\beta}\right) I_{C_1}$$

Applying KVL for transistor Q_1 emitter loop, we have

$$V_{CC} - I_1 R_{C_1} - V_{BE} - I_{E_1} R_{E_1} - V_{EE} = 0$$

Substituting the values, we get

$$6 - (\beta + 2)\, I_{B_1} \times (10 \times 10^3) - 0 \cdot 6 - (\beta + 1)\, I_{B_1} \times (1 \cdot 4 \times 10^3) - (-6) = 0$$

or $$I_{B_1} = \frac{11 \cdot 4}{10^4 \times (\beta + 2) + (1 \cdot 4 \times 10^3)(\beta + 1)} = \frac{11 \cdot 4}{10^4 \times (20 + 2) + (1 \cdot 4 \times 10^3)(20 + 1)} \quad (\because \beta = 20)$$

or $$I_{B_1} \simeq 0 \cdot 045 \text{ mA}$$

$$I_1 = (\beta + 2)\, I_{B_1} = (20 + 2) \times 0 \cdot 045 = \mathbf{1 \cdot 005 \text{ mA}}$$

$$I_2 = I_{C_1} = I_{C_1} = \beta\, I_{B_1} = 20 \times 0 \cdot 045 = \mathbf{0 \cdot 9 \text{ mA}}$$

When β is large, then I_B is negligibly small. Now,

$$I_1 \simeq I_2 \simeq I_{C_1} = \beta\, I_{B_1}$$

or $$I_{B_1} = \frac{11 \cdot 4}{10^4 (\beta + 2) + (1 \cdot 4 \times 10^3)(\beta + 1)} = \frac{11 \cdot 4}{10^4 \beta + 1 \cdot 4 \times 10^3 \beta}$$

or $$I_{B_1} = \frac{1}{\beta} \text{ mA}$$

and $$I_{C_1} = I_1 + I_2 = \beta\, I_{B_1} = \beta \times \frac{1}{\beta} = \mathbf{1 \text{ mA}}$$

Scanned with CamScanner

Example 6. *Figure* (19·59) *shows the differential amplifier using transistors with* $\beta = 100$.

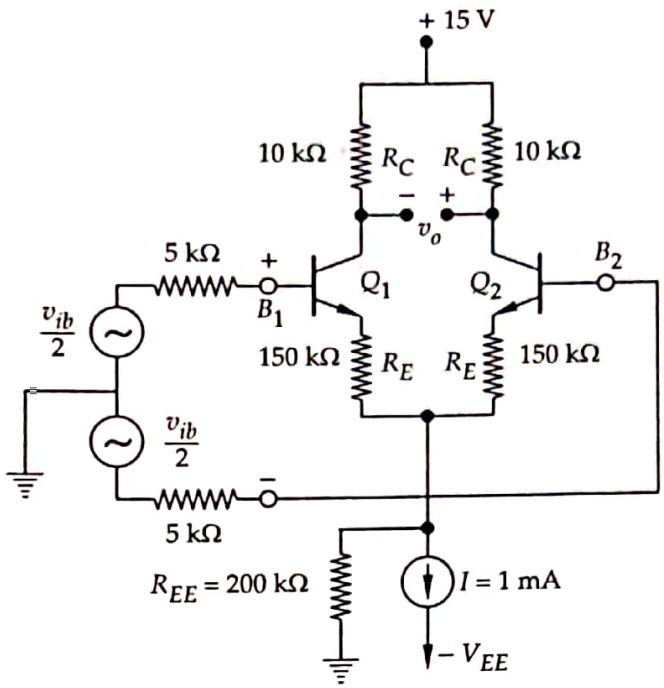

Fig. 19·59 Differential amplifier using transistors

Evaluate the following:

(a) The input differential resistance (R_{id}).
(b) The overall differential voltage gain (v_0/v_{ib}).
(c) The worst-case common-mode gain if the two collector resistances are accurate to within ± 1 %.
(d) The CMRR *in* dB.
(e) The input common-mode resistance (assuming that early voltage) $V_A = 100$ V.

(a) Each transistor is biased at an emitter current of 0·5 mA.

The emitter resistance is given by

$$r_{e1} = r_{e2} = \frac{V_T}{I_E} = \frac{25 \text{ mV}}{0{\cdot}5 \text{ mA}} = 50\,\Omega$$

The input differential resistance can be obtained as

$$R_{id} = 2(\beta + 1)(r_e + R_E)$$
$$= 2(101)(50 + 150) = 40 \text{ k}\Omega$$

(b) The voltage gain from the signal source to the base of Q_1 and Q_2 is

$$\frac{v_{id}}{v_{ib}} = \frac{R_{id}}{R_{ib} + R_{id}} = \frac{40 \text{ k}\Omega}{(5 \text{ k}\Omega + 5 \text{ k}\Omega) + 40 \text{ k}\Omega} = 0{\cdot}8$$

The voltage gain from the bases to the output is

$$\frac{v_0}{v_{id}} = \frac{\text{Total resistance of collectors}}{\text{Total resistance in the emitter}} = \frac{2R_C}{2(r_e + R_E)}$$

$$= \frac{2 \times (10 \times 10^3)}{2(50 + 150)} = 50$$

The overall differential voltage gain can be found as

$$A_d = \frac{v_0}{v_{ib}} = \frac{v_{id}}{v_{ib}} \times \frac{v_0}{v_{id}} = 0{\cdot}8 \times 50 = 40$$

Scanned with CamScanner

(c) $A_{CM} = \dfrac{R_C}{2R_{EE}}\left(\dfrac{\Delta R_C}{R_C}\right)$

$\Delta R_C = 0{\cdot}02\, R_C$ in the worst case. Thus

$$A_{CM} = \frac{10\ \text{k}\Omega}{2\times 200\ \text{k}\Omega}\times 0{\cdot}02 = 5\times 10^{-4}$$

(d) $\text{CMRR in dB} = 20\log\left|\dfrac{A_d}{A_{CM}}\right| = 20\log\left|\left(\dfrac{40}{5\times 10^{-4}}\right)\right| = 98\ \text{dB}$

(e) $r_0 = \dfrac{V_A}{(I/2)} = \dfrac{100}{(0{\cdot}5\times 10^{-3})} = 200\ \text{k}\Omega$

$$(R_i)_{CM} = (\beta+1)\left(R_{EE} \parallel \frac{r_0}{2}\right) = (101)\,[200\ \text{k}\Omega \parallel 100\ \text{k}\Omega] = 6{\cdot}7\ \text{m}\Omega$$

Example 7. *For the differential amplifier of fig.* (19·60), *let* $I = 1$ mA, $V_{CC} = 5$ V, $v_{CM} = -2$ V, $R_C = 3$ kΩ *and* $\beta = 100$. *Assume that BJTs has* $v_{BE} = 0{\cdot}7$ V *at* $i_C = 1$ mA. *Find the voltage at emitters and at the outputs.*

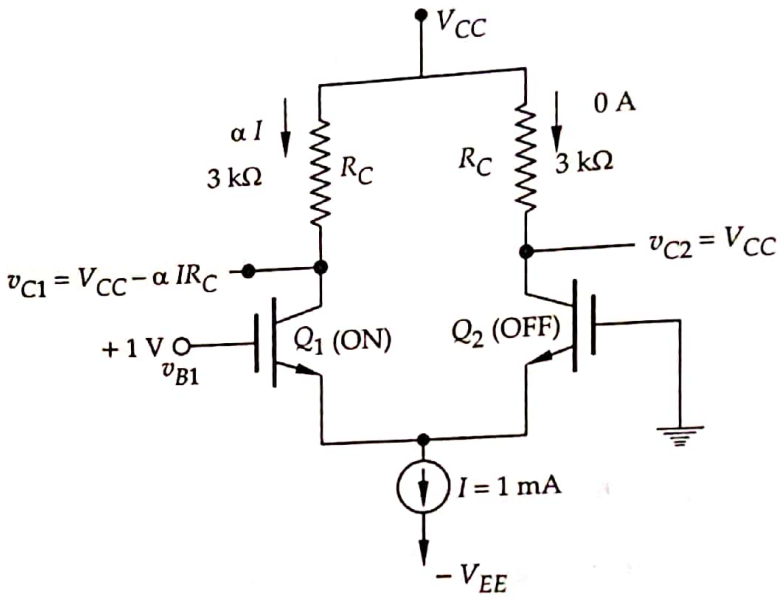

Fig. 19·60 Differential amplifier

For input condition Q_1 is ON and Q_2 is OFF.

$$i_{C_1} = \alpha I = 1\times 1\ \text{mA} = 1\ \text{mA}$$

$$v_{BE1} \cong 0{\cdot}7\ \text{V}$$

$$v_E = V_B - v_{BE} = 1 - 0{\cdot}7 = 0{\cdot}3\ \text{V}$$

$$v_{C_1} = V_{CC} - i_{C_1} R_C = 5 - (1\times 10^{-3})\times(3\times 10^{3}) = 2\ \text{V}$$

and $v_{C_2} = V_{CC} - i_{C_2} R_C = 5 = 0 = 5\ \text{V}$

Scanned with CamScanner