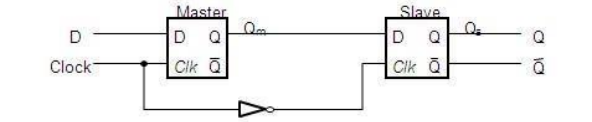
Flip-Flops

Flip-Flops

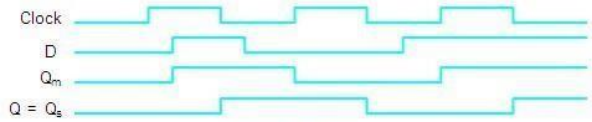
- A **flip-flop** is a storage element based on the gated latch principle
- It can have its output state changed only on the edge of the controlling clocksignal
- We consider two types:

- **Edge-triggered flip-flop** is affected only by the input values present when theactive edge of the clock occurs
- **Master-slave flip-flop** is built with two gatedlatches
- The master stage is active during half of the clock cycle, and the slave stage is active during the other half.
- The output value of the flip-flop changes on the edge of the clock that activates the transfer into the slave stage.

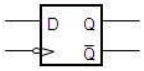
Master-Slave D Flip-Flop



(a) Circuit

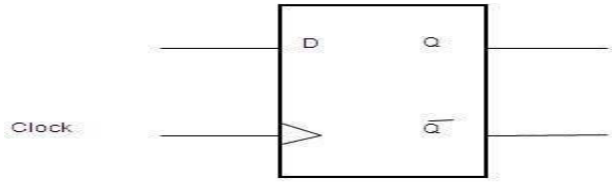


(b) Timing diagram



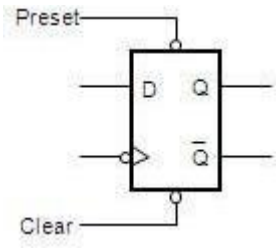
(c) Graphical symbol

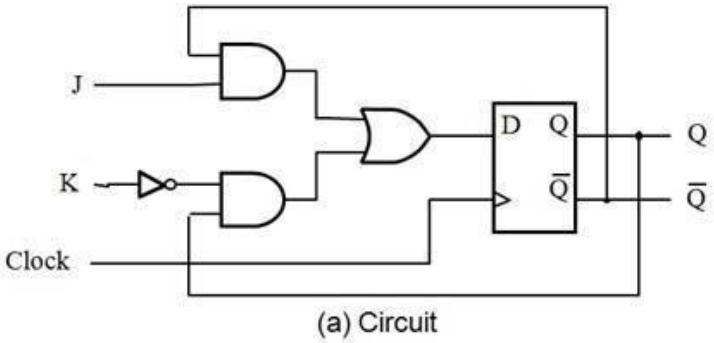
A Positive-Edge-Triggered D Flip-Flop



Graphical symbol

Master-Slave D Flip-Flop with *Clear* and *Preset*

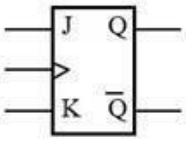




(a) Circuit

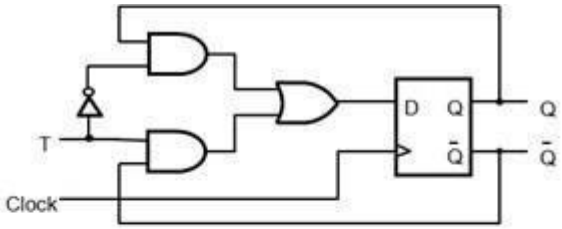
J	K	Q (t+1)
0	0	Q (t)
0	1	0
1	0	1
1	1	$\overline{Q}$ (t)

(b) Characteristic table



(c) Graphical symbol

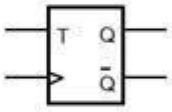
T Flip-Flop



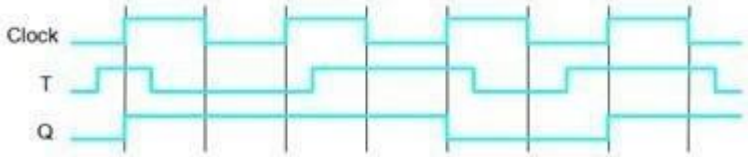
(a) Circuit

T	Q(t + 1)
0	Q(t)
1	Q(t)

(b) Characteristic table



(c) Graphical symbol



(d) Timing diagram

Excitation Tables

Previous State -> Present State	D
0 -> 0	0
0 -> 1	1
1 -> 0	0
1 -> 1	1

Previous State -> Present State	J	K
0 -> 0	0	X
0 -> 1	1	X
1 -> 0	X	1
1 -> 1	X	0

Previous State -> Present State	S	R
0 -> 0	0	X
0 -> 1	1	0
1 -> 0	0	1
1 -> 1	X	0

Previous State -> Present State	T
0 -> 0	0
0 -> 1	1
1 -> 0	1
1 -> 1	0