OXIDATION

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INTRODUCTION

- Oxidation refers to the chemical process of reaction of silicon with oxygen to form silicon di-oxide.
- In an IC fabrication, the silicon dioxide has following uses:-
  - To serve as mask against implant or difussion atom into silicon.
  - It is used for surface protection.
  - To isolate one device from another because of its dielectric properties and also between the conducting layers.
  - It is used for capping doped film to prevent loss of dopant.

OXIDE GROWTH

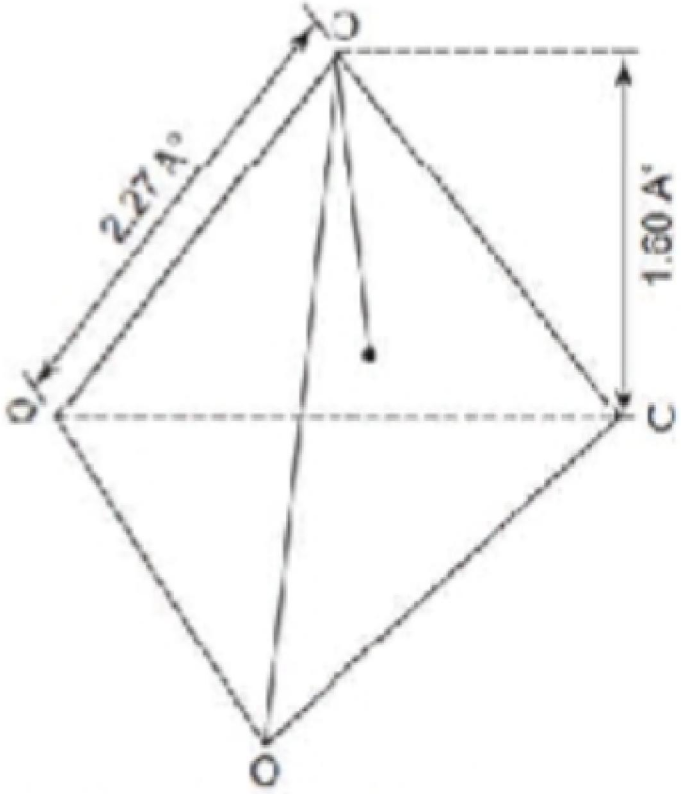
- The silicon surface easily reacts with oxygen so an oxide layer is rapidly formed when the wafer is exposed to oxygen. The following reaction take place

$$Si + O_2 \rightarrow SiO_2 \text{ in oxygen}$$

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \text{ in water vapour}$$

- The structure of thermally grown silicon dioxide is silicon ion surrounded tetrahedrally by 4 oxygen atoms as shown in fig. The silicon-oxygen internuclear distance is 1.6 A and oxygen internuclear distance is 2.27 A.

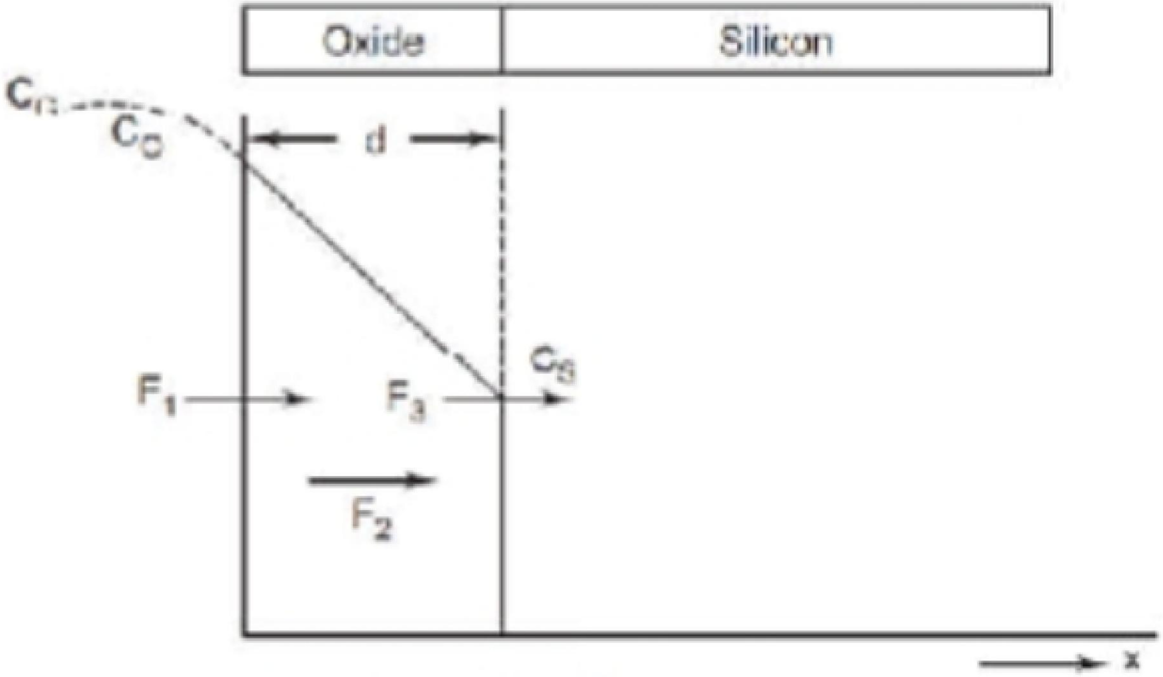
OXIDE GROWTH



SILICON OXIDATION MODEL

- Deal and Grove's model describe the kinetics of silicon oxidation. The model is generally valid for temperature between 700 and 1300 degree C, partial pressure between 0.2 and 1 atm and oxide thickness between 300 to 20,000 A for oxygen and water ambient.
- Figure shows the silicon substrate covered by an oxide layer that is in contact with the gas phase.
- The oxidizing species:
  - Are transported from the bulk of the gas phase to the gas oxide interface with flux F1.
  - are transported across the existing oxide toward the silicon with flux F2 and
  - React of Si-SiO2 interface with silicon with flux F3.

SILICON OXIDATION MODEL



Basic Model for Thermal Oxidation

SILICON OXIDATION MODEL

- For steady state
  - F1=F2=F3

- The gas phase flux F1 can be linearly approximated by assuming that the flux of oxiidant from the bulk of the gas phase to gas oxide interface is proportional to the difference between the oxidant concentration in the bulk gas C*and the concentration gradient to the oxide surface Co.
  - F1=hg (C*-Co)

Where hg is the gas phase mass interface coefficient

SILICON OXIDATION MODEL

- The flux of the oxidizing species across the oxide is taken to follow flick's law at any point in the oxide layer following the steady state exemptions, F2 must be same at any point within the oxide, resulting in

$$F_2 = D\frac{dc}{dx} = \frac{D(C_O - C_S)}{x}$$

- Where D is the diffusion coefficient, Cs is the oxidizing species concentration in the oxide adjacent to oxide-silicon interface, Co is the equilibrium concentration in the oxide at the outer surface and x is the oxide thickness.

SILICON OXIDATION MODEL

- Assuming that the flux corresponding to Si-SiO2 interface reaction is proportional to Cs,

$$F_3 = kC_S.$$

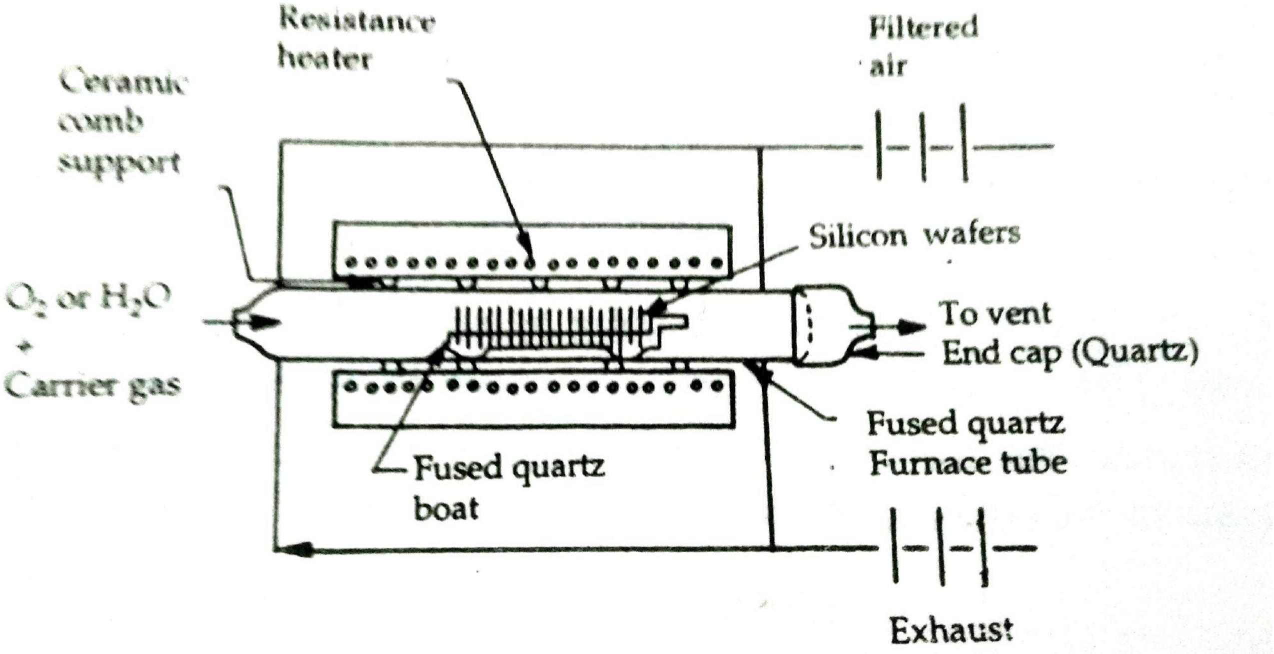
- Where Ks is the rate constant of chemical surface reaction for silicon oxidation
- After setting F1=F2=F3, a steady state condition, and solving simultaneous equation, expression for Cs and Co can be obtained.

SILICON OXIDATION MODEL

- When diffusivity is very small, Cs->0 and Co -> C*.This case is called diffusion controlled case. It results from the flux of oxidant through the oxide being small(due to D being small) compare to the flux corresponding Si-SiO2 interface reaction. Hence, the oxidation rate depend on the supply of oxidant to the interface, as opposed to the reaction at the interface.
- In the second limiting case, where Di lrge,Cs=Co. This is called reaction controlled case, because an abundant supply of oxidants is provided at Si-SiO2 interface, and the oxidation state is controlled by the reaction rate constant Ks and by Cs.

OXIDATION SYSTEM

- Thermal oxidation has been a principle technique in silicon IC technology. Schematic cross section of a resistance heated oxidation furnance is shown in Fig.below.



OXIDATION SYSTEM

- It is described below:
  - A cylindrical fused quartz tube containing the wafer is held vertically in a slotted quartz boat.
  - The wafer are exposed to a source of either pure dry oxygen or pure water vapour.
  - The loading end of the furnance tube enters into a vertical flow hood where a filtered flow of air is maintained.
  - The hood reduce dust and particle matter in air surrounding the wafer and minimize the contamination at the time of wafer loading.
  - The furnace temperature is maintained between 900 to 1200 degree C and gas flow rate is maintained at 1cm/sec.
  - Microprocessor are used to regulate the gas flow sequence to control the automatic insertion and removed of Si wafer to control the temp. etc.

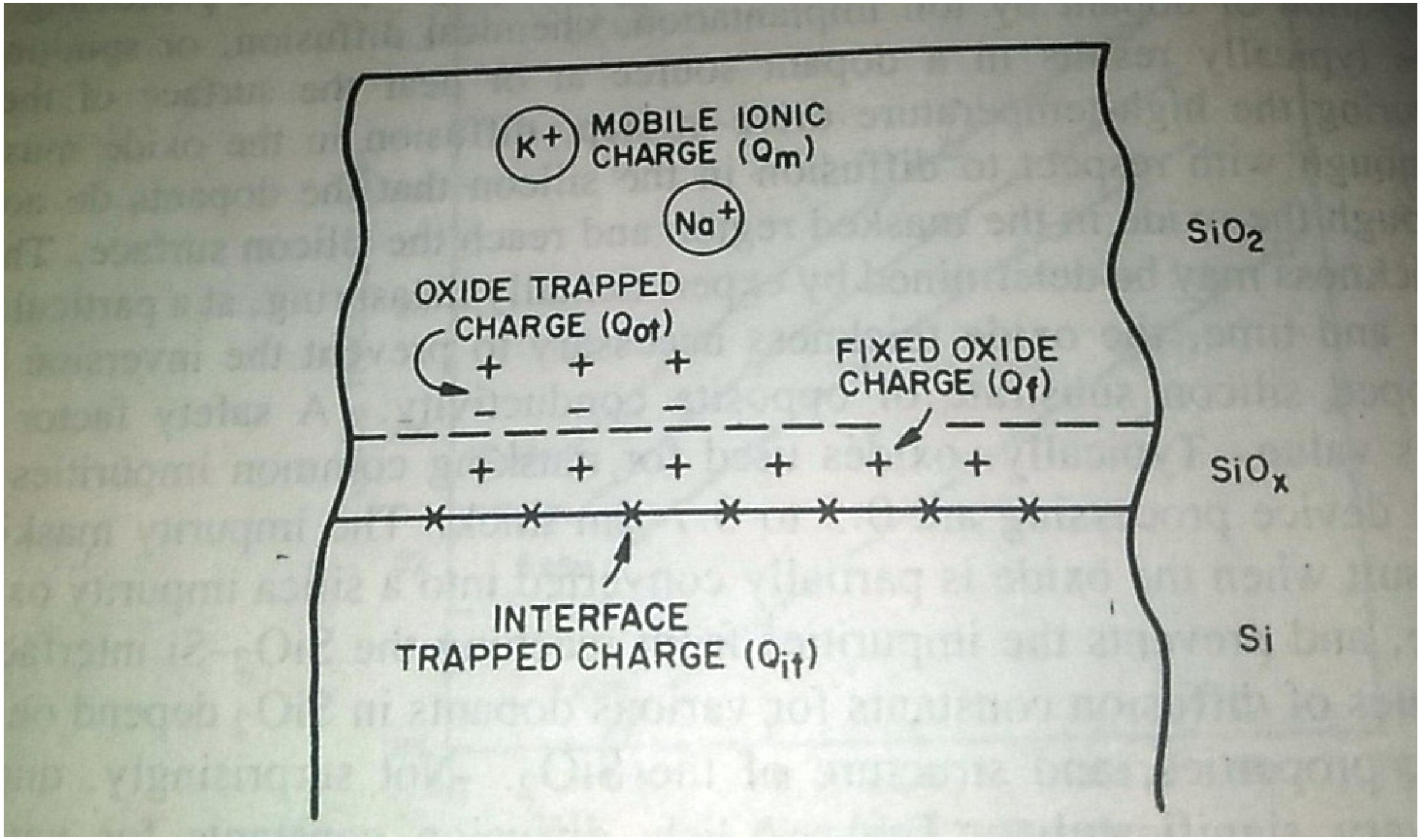
OXIDE PROPERTIES

- **Oxide as a Mask**
  - The silicon dioxide layer grown on silicon act as a mask against the diffusion of dopant atom at higher temperature.
  - The required thickness of the oxide layer is determined at the time of experiment .Usually 0.5 to 0.7 micron thick oxide are used to mask common impurities in silicon.
  - The common impurities used are phosphorus, arsenic and antimony for n type doping and boron for p type doping. All the impurities have small diffusion coefficient in oxide so that SiO2 serve as effective mask for them.

OXIDE PROPERTIES

- **Charges in Oxide**
  - There is a transition region at the Si-SiO2 interface in terms of position and stochiometry between the crystalline silicon and amorphous silica. There are different charges and traps in oxidized silica.
  - Some charges are there in transition region also. Any charge present at interface induces a charge in the underlying silicon which is of different polarity.
  - This results in a deviation of MOS characteristics and thus create functional problems. General type of charges in the thermally oxidized silicon are shown in Fig and are described as:

OXIDE PROPERTIES



OXIDE PROPERTIES

- **Interface trapped charges Qit:**

They are located at the Si-SiO2 interface.They have energy states in the silicon forbidden gap and can electrically interact with underlying silicon. These charges are thought to result from several sources, including structural defects related to the oxidation process, metallic impurities, or bond breaking processes.

A low temperature hydrogen anneal(450 degree) effectively neutralizes interface-trapped charge.

The density of these charges is usually expressed in term of unit area and energy in the silicon bandgap (number/cmsq-eV) and can be determined by capacitance-voltage and conductance-voltage technique.

Experimental results show a density of 10^10/cm^2 of these charges.

OXIDE PROPERTIES

- **Fixed oxide charges:**

Located at 30 angstrom of Si-SiO2 interface and these cannot be charged or discharged.

Density range 10^10 to 10^12 /cm^2, depending on oxidation and annealing conditions as well as orientation.

These can be considered as sheet of charges at the Si-SiO2 interface and its value can be determined by the Capacitance-Voltage (C-V) analysis technique.

Temperature and ambient used during oxidation determine the density of their charges.

OXIDE PROPERTIES

- **Mobile ionic charges (Qm):**

These charges are formed due to alkali ion such as sodium,potassium, and lithium in the oxide as well as to negative ion and heavy metals. The alkali ions are mobile even at room temperature, when electric fields are present.

Densities :10^10 to 10^12 per cm^2

They occur due to processing material, chemicals, ambient and handling.

To minimize this charges, the furnance tube should be cleaned in a chloride ambient, gettering with phosphosilicate glass or masking layer of silicon nitride may be used.

Measurement can be made by C-V technique, but these alkali ions are present at various place in the oxide, the MOS capacitor is subjected to a temperature bias stress test which is compared to standard C-V plot.

OXIDE PROPERTIES

- **Oxide trapped charges Qot**

They can be positive or negative due to holes or electrons trapped in the bulk of oxide .This charges associated with defects in the SiO2, may result from ionizing radiation, avalanche injection or high currents in the oxide.

It can be annealed out by low temperature treatment.

Densities:10^9 – 10^11 /cm^2

C-V technique can be used to measure the charges.

OXIDE PROPERTIES

- **Stress in oxide layer.**

To know the amount of stress in a layer is important as higher stress result in the layer damage and may introduce defected in underlying layers.

Stress values of about 3x10^9 dynes/cm^2 at room temperature which are due to different coefficient of thermal expansion of silicon and silicon dioxide.

So stress free oxide growth is usually preferred.

During device processing, windows are cut into the oxide , resulting in a complex a stress distribution. Exceedingly high stress levels can occur at these discontinuities. Such stresses would typically be releived by plastic flow or other stress-relief mechanism.