(ii) ALU: The control unit controls the operations of the ALU by a set of control signals. These signals activate various logic circuits and gates within the ALU.

(iii) System Bus: The control unit sends control signals out onto the control lines of the system bus. (e.g. memory READ).

(3) The control unit must maintain knowledge of where it is in the instruction cycle.

- Using this knowledge, and by reading all of its inputs, the control unit emits a sequence of control signals that causes micro-operations to occur.

(4) It uses the clock pulse to time the sequence of events,

(5) The control unit is the engine that runs the entire computer.

- It does this based only on knowing the instructions to be executed and the nature of the results of arithmetic and logical operations.

- It never gets to see the data being processed or the actual results produced.
- It controls everything with a few control signals to points within the processor and a few control signals to the system bus.

eg: Consider Fetch Sub Cycle.

Note: For simplicity, the data and control paths for incrementing the PC & for loading the fixed addresses into the PC & MAR are not shown.

	Micro operation	Active Control Signals	
t_1 :	MAR ← PC	C_2	
t_2 :	MBR ← Memory PC ← (PC) + 1	C_5, C_R	C_R - read control signal to system bus
t_3 :	IR ← (MBR)	C_4	

Step 1: The first step is to transfer the content of the PC to the MAR.
The control unit does this by activating the control signals that opens the gates b/w the bits of the PC & the bits of the MAR.

Step 2: The next step is to read a word from memory into the MBR and increment the PC.

Step 3: Following this, the control unit sends a control signal that opens the gates b/w the MBR and the IR.