

**Design a Half Adder circuit using
NAND Gates**

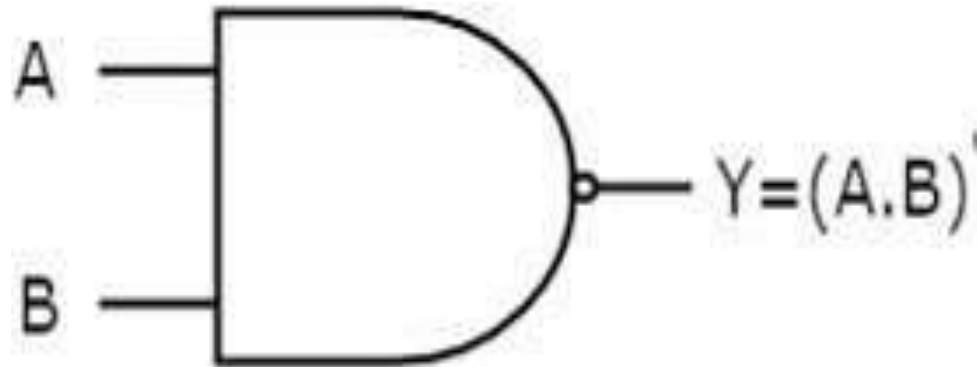
**Design a Half Adder circuit using
NOR Gates**

NAND Gate

- It is a digital circuit that has two or more inputs and produces an output, which is the inversion of logical AND of all those inputs.
- Logic NAND Gates are available using digital circuits to produce the desired logical function and is given a symbol whose shape is that of a standard AND gate with a circle, sometimes called an "inversion bubble" at its output to represent the NOT gate symbol with the logical operation of the NAND gate.

NAND Gate

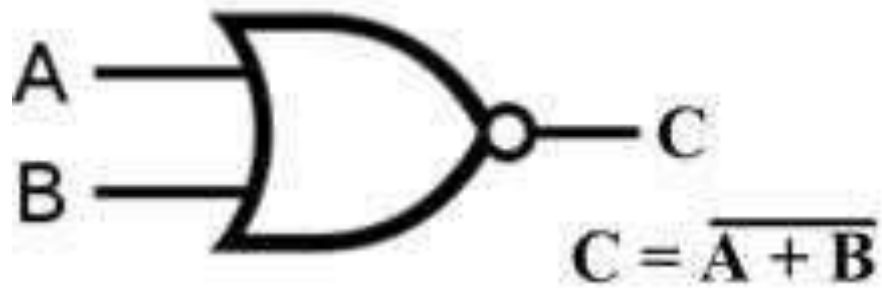
- Boolean Expression $Y = (A.B)'$
- "If either A or B are NOT true, then Y is true"



NOR GATE

- The NOR gate is also a universal gate. So, we can also form all the basic gates using the NOR gate. The NOR gate is the combination of the NOT-OR gate. The output state of the NOR gate will be high only when all of the inputs are low. Simply, this gate returns the complement result of the OR gate.
- The logical or Boolean expression for the NOR gate is the complement of logical multiplication of inputs denoted by the plus sign as
- $(A+B)'=Y$
- The value of Y will be true when all of its inputs are set to 0

NOR GATE



TRUTH TABLE

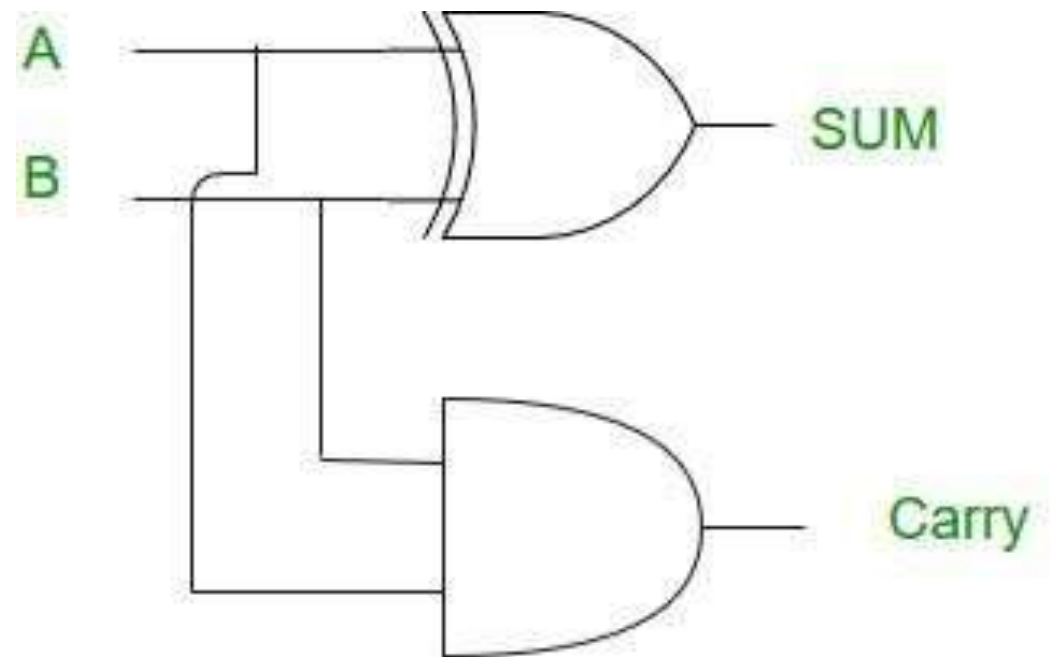
| INPUT | | OUTPUT |
|-------|---|---------|
| A | B | A NOR B |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

Half Adder in Digital Logic

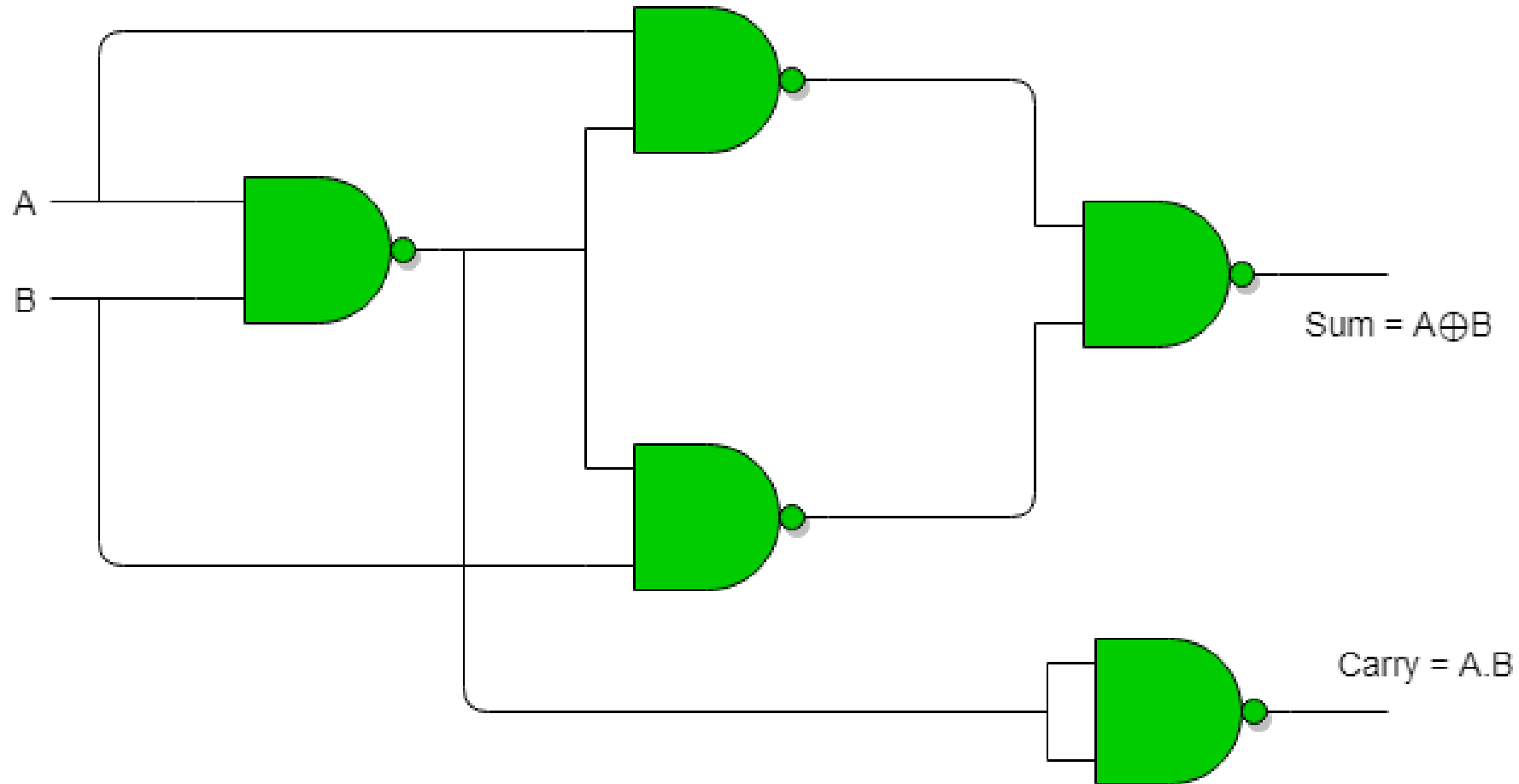
- Half adder is the simplest of all adder circuits. Half adder is a combinational arithmetic circuit that adds two numbers and produces a sum bit (s) and carry bit (c) both as output. The addition of 2 bits is done using a combination circuit called a Half adder. The input variables are augend and addend bits and output variables are sum & carry bits. A and B are the two input bits.

Half Adder in Digital Logic

let us consider two input bits A and B, then sum bit (s) is the X-OR of A and B. it is evident from the function of a half adder that it requires one X-OR gate and one AND gate for its construction.



Implementation of Half Adder using NAND gates



Implementation of Half Adder using NOR GATE

