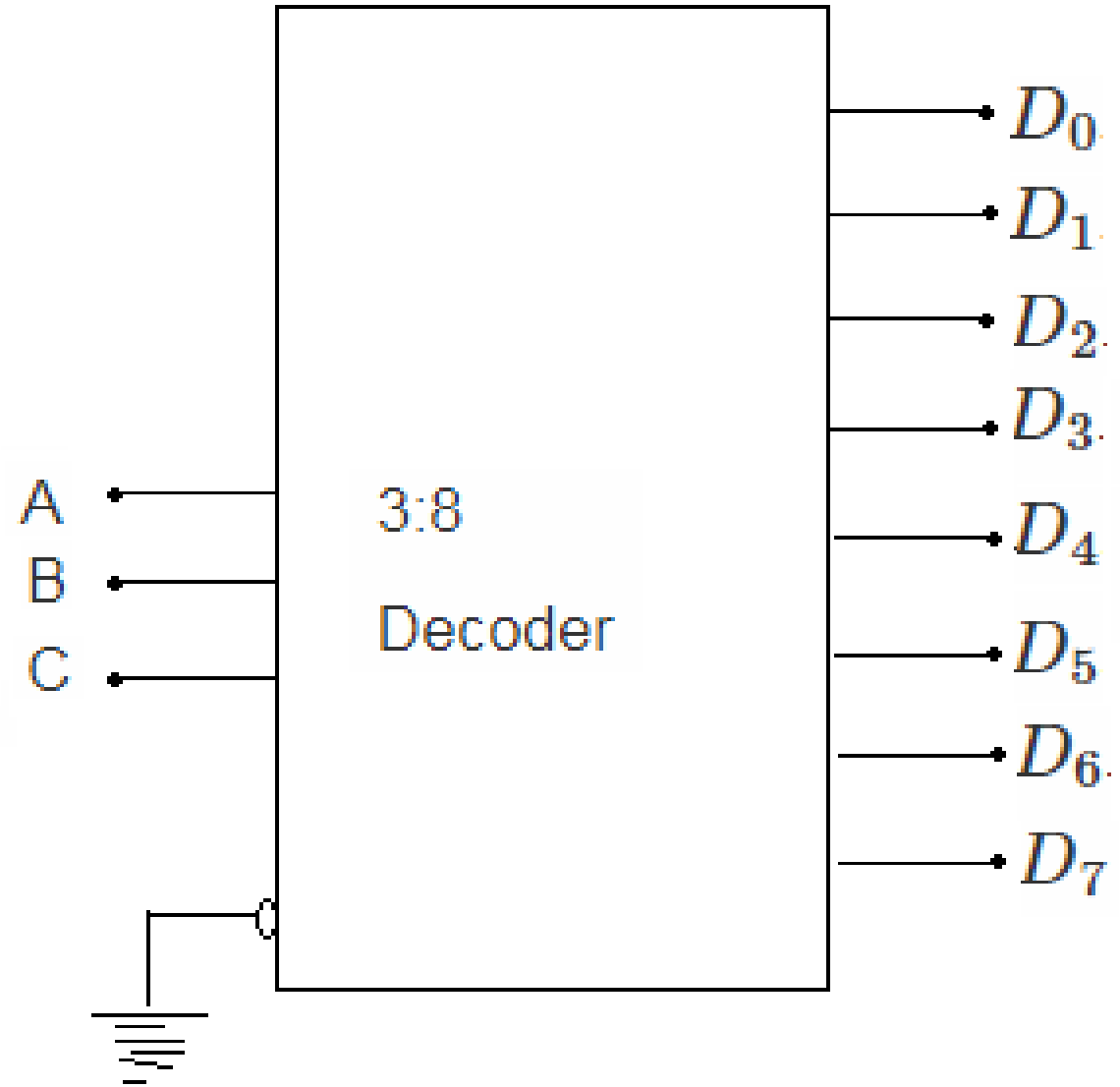
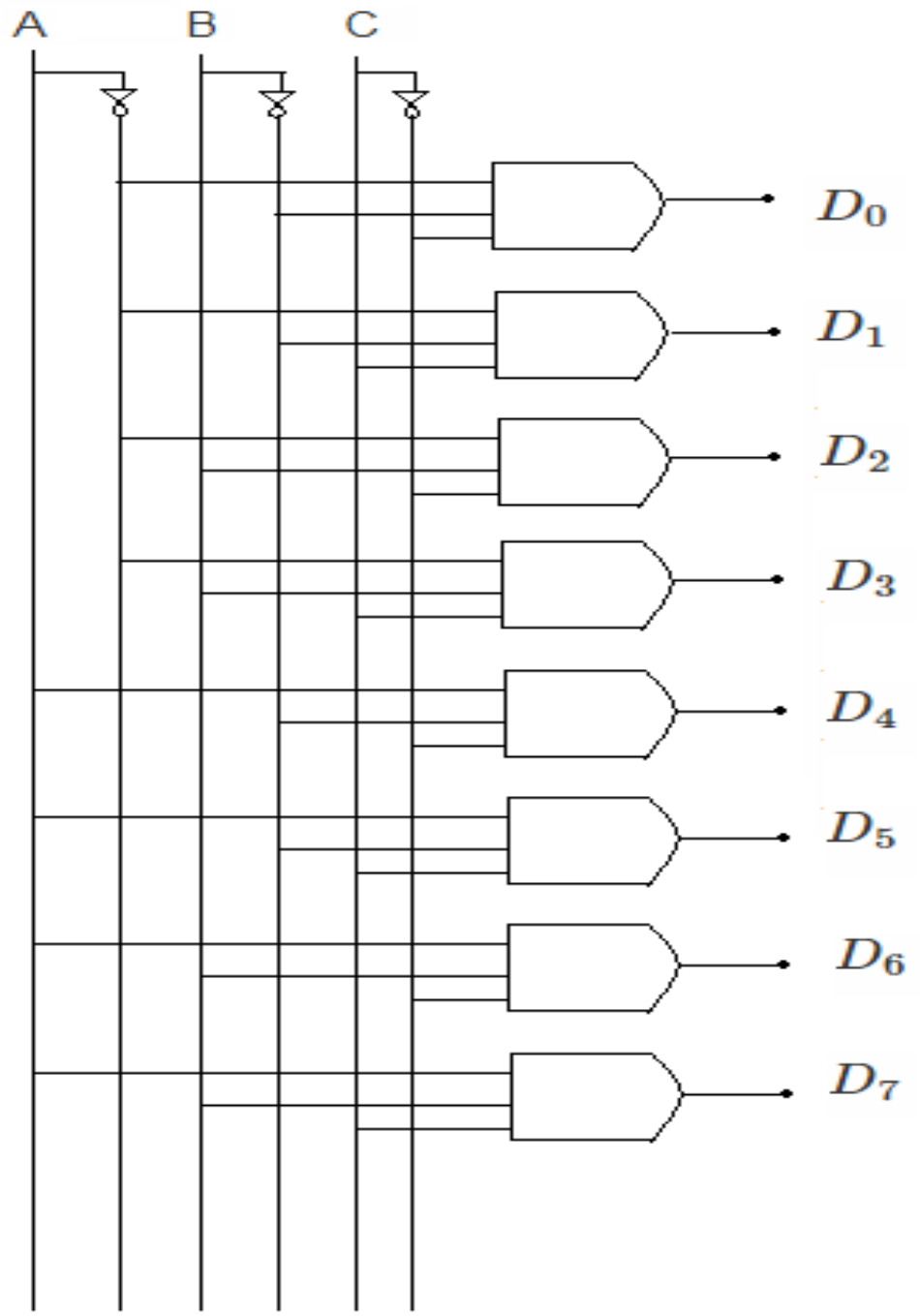
3*8 BINARY DECODER

- A 3*8 decoder has three inputs (A, B, C) and eight outputs (D0 to D7).
- Based on the 3 inputs one of the eight outputs is selected.
- The truth table for 3 to 8 decoder is shown in the below table.
- From the truth table, it is seen that only one of eight outputs (D0 to D7) is selected based on three select inputs.
- From the truth table, the logic expressions for outputs can be written as follows:



- It is also called a binary-to-octal decoder since the inputs represent 3-bit binary numbers and the outputs represent the eight digits in the octal number system.

Inputs			Outputs							
x	y	z	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1



$$D_0 = \bar{A}\bar{B}\bar{C}, \quad D_1 = \bar{A}\bar{B}C, \quad D_2 = \bar{A}B\bar{C},$$

$$D_3 = \bar{A}BC, \quad D_4 = A\bar{B}\bar{C}, \quad D_5 = A\bar{B}C,$$

$$D_6 = AB\bar{C}, \quad D_7 = ABC$$

Using the above expressions, the circuit of a 3 to 8 decoder can be implemented using three NOT gates and eight 3-input AND gates

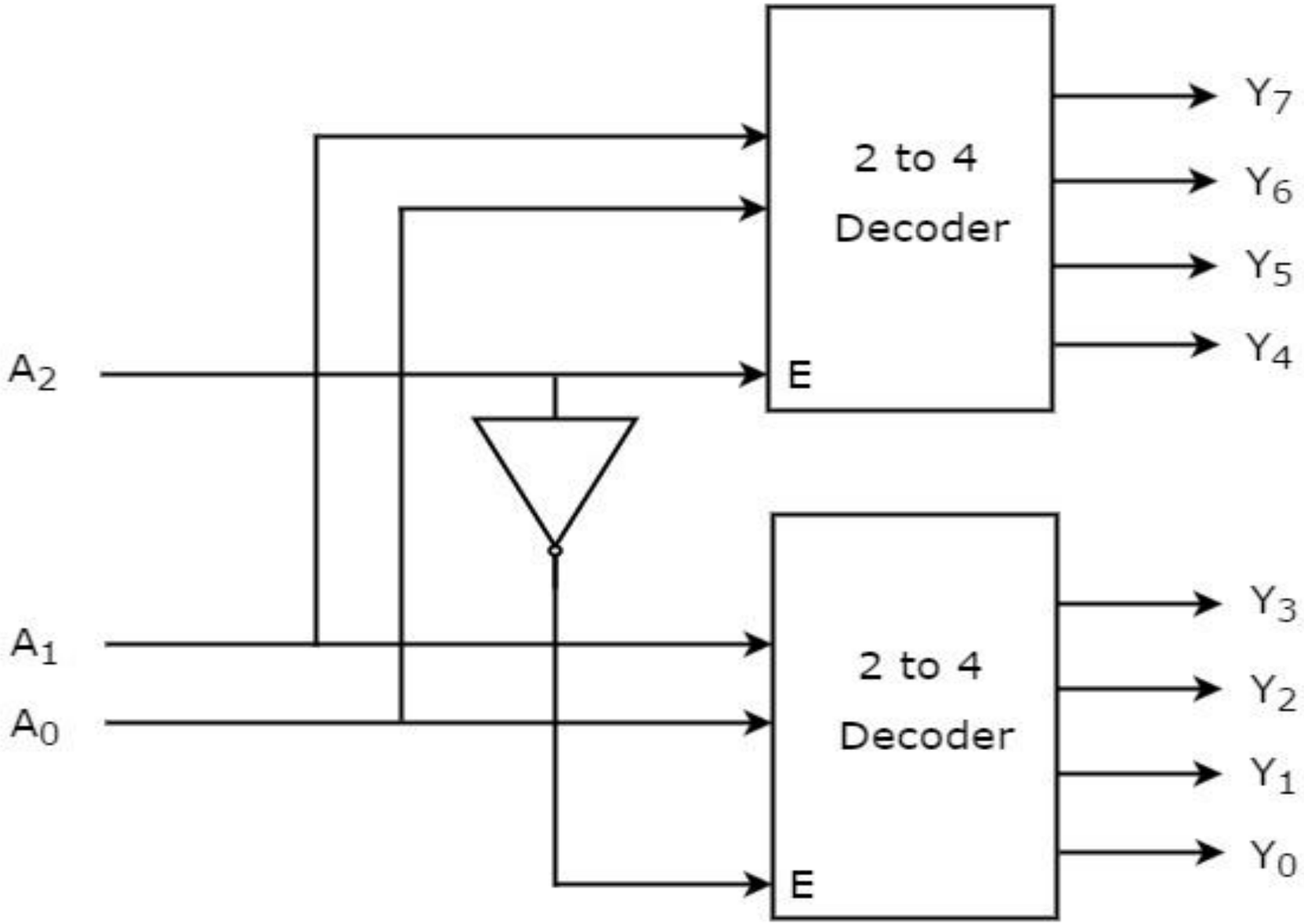
- The three inputs A, B, and C are decoded into eight outputs, each output representing one of the midterms of the 3-input variables.
- The three inverters provide the complement of the inputs and each one of the wight AND gates generates one of the midterms.
- This decoder can be used for decoding any 3-bit code to provide eight outputs, corresponding to eight different combinations of the input code.
- This is also called a 1 of 8 decoder since only one of eight output lines is HIGH for a particular input combination.

3*8 DECODER USING TWO 2*4 DECODER

In this section, let us implement **3 to 8 decoder using 2 to 4 decoders**. We know that 2 to 4 Decoder has two inputs, A_1 & A_0 and four outputs, Y_3 to Y_0. Whereas, 3 to 8 Decoder has three inputs A_2, A_1 & A_0 and eight outputs, Y_7 to Y_0.

.

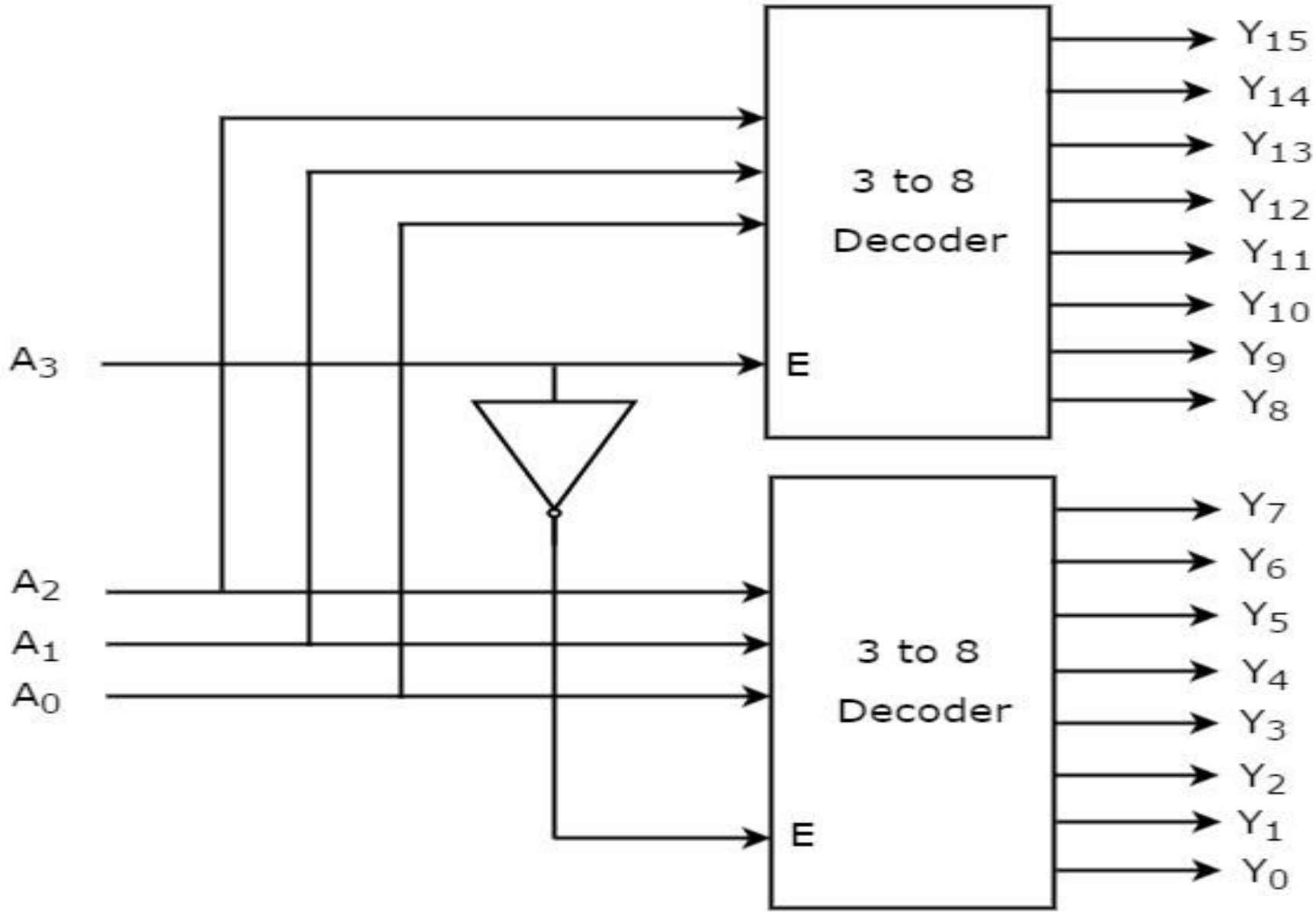
The parallel inputs A_1 & A_0 are applied to each 2 to 4 decoder. The complement of input A_2 is connected to Enable, E of lower 2 to 4 decoder in order to get the outputs, Y_3 to Y_0. These are the **lower four min terms**. The input, A_2 is directly connected to Enable, E of upper 2 to 4 decoder in order to get the outputs, Y_7 to Y_4. These are the **higher four min terms**.


2 to 4
Decoder
E
2 to 4
Decoder
E
A2
A1
A0
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0

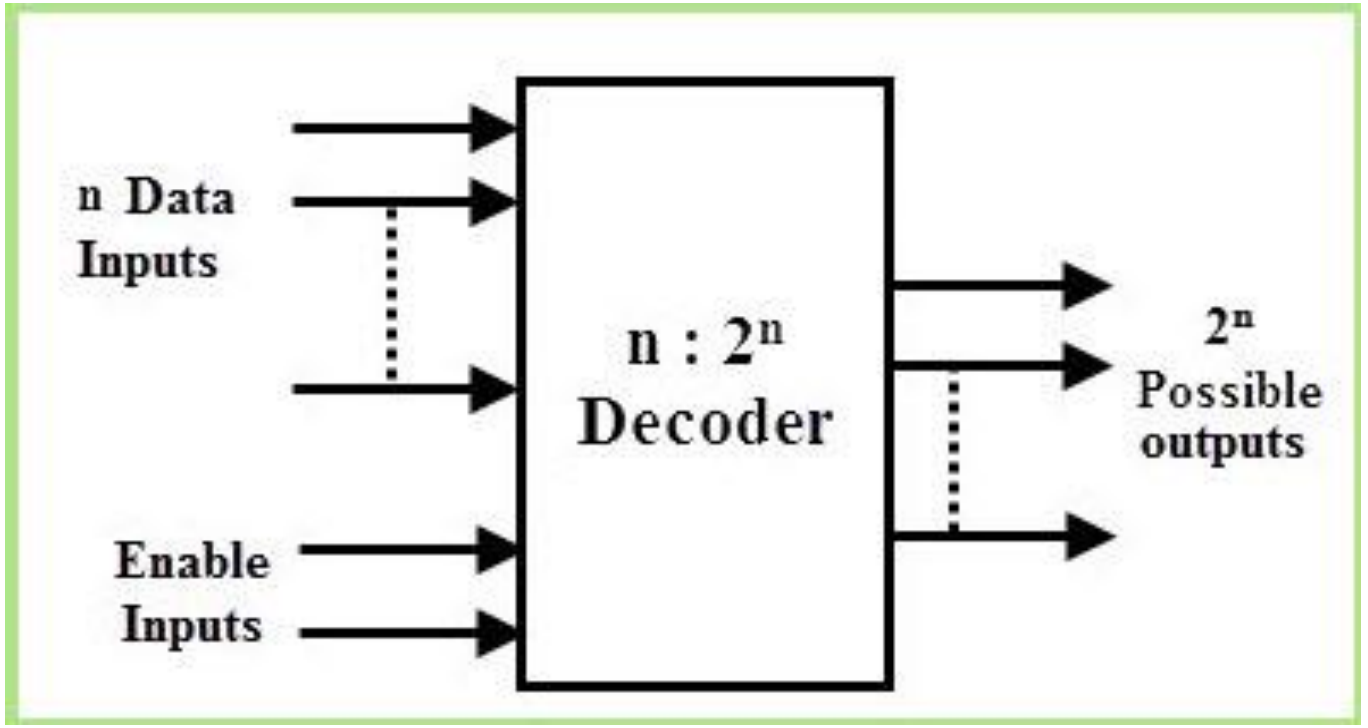
4*16 BINARY DECODER

In this section, let us implement **4 to 16 decoder using 3 to 8 decoders**. We know that 3 to 8 Decoder has three inputs A_2, A_1 & A_0 and eight outputs, Y_7 to Y_0. Whereas, 4 to 16 Decoder has four inputs A_3, A_2, A_1 & A_0 and sixteen outputs, Y_{15} to Y_0

Therefore, we require two 3 to 8 decoders for implementing one 4 to 16 decoder. The **block diagram** of 4 to 16 decoder using 3 to 8 decoders is shown in the following figure.


3 to 8
Decoder
E
3 to 8
Decoder
E
A3
A2
A1
A0
Y15
Y14
Y13
Y12
Y11
Y10
Y9
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0

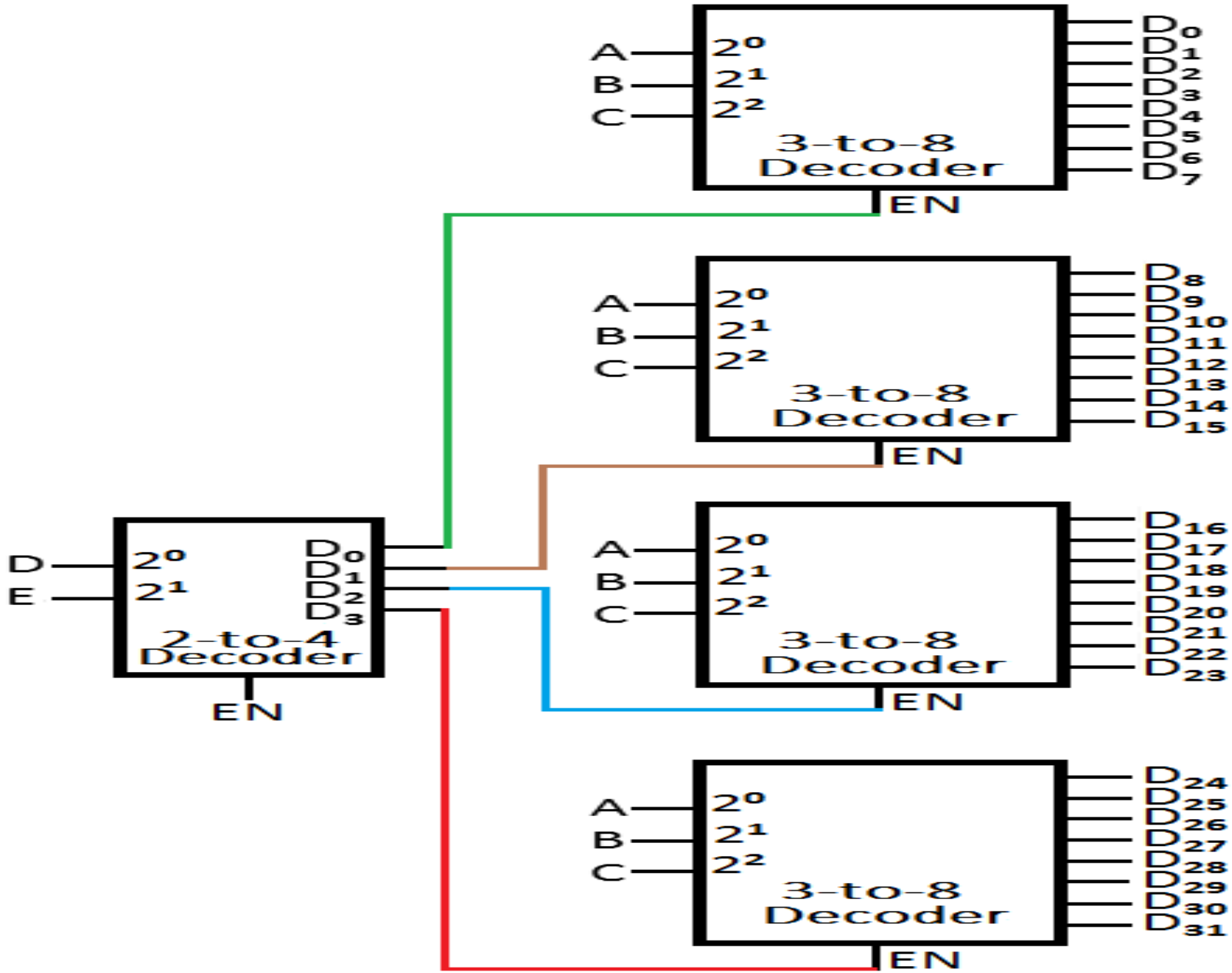
The parallel inputs A_2, A_1 & A_0 are applied to each 3 to 8 decoder. The complement of input, A3 is connected to Enable, E of lower 3 to 8 decoder in order to get the outputs, Y_7 to Y_0. These are the **lower eight min terms**. The input, A_3 is directly connected to Enable, E of upper 3 to 8 decoder in order to get the outputs, Y_{15} to Y_8. These are the **higher eight min terms**.

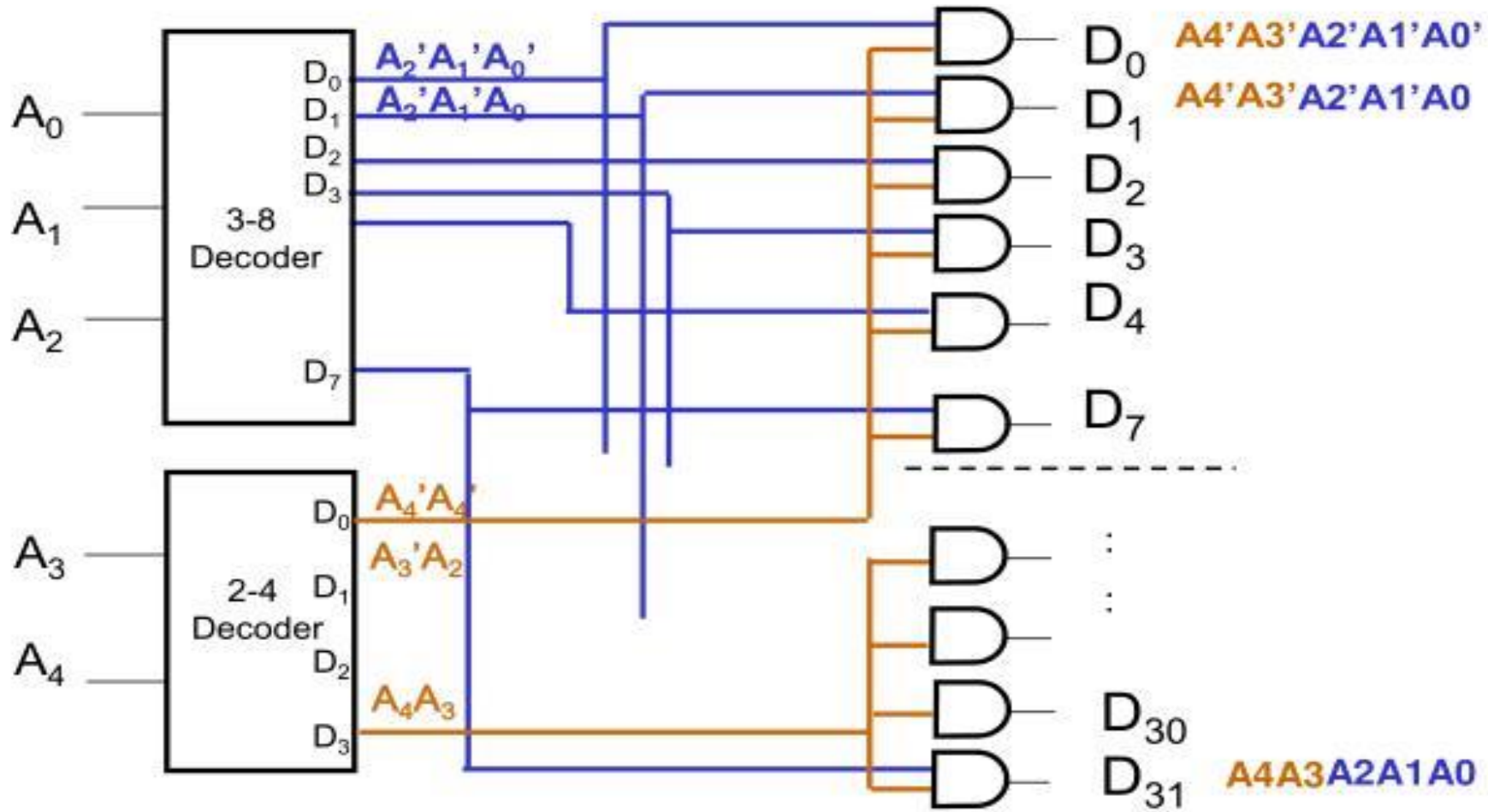


5*32 BINARY DECODER

In **5* 32 Decoder** we have 5 input lines and 32 output lines and will just select one output line based on various input combinations.
We can design a 5*32 decoder using one 2*4 decoder and four 3*8 decoder

- When A = 0 , B = 0 ,C = 0, DE(any 00 or 01 or 10 or 11)
- D1 Decoder is selected.
- When A = 0 , B = 0,C =1 , DE(any 00 or 01 or 10 or 11)
- D2 Decoder is selected.
- When A = 0 , B = 1 ,C=0, DE(any 00 or 01 or 10 or 11)
- D3 Decoder is selected.
- When A = 0 , B = 1,C = 1 ,DE(any 00 or 01 or 10 or 11)
- D4 Decoder is selected.


D
E
2⁰
2¹
D₀
D₁
D₂
D₃
2-to-4
Decoder
EN
A
B
C
2⁰
2¹
2²
3-to-8
Decoder
EN
D₀
D₁
D₂
D₃
D₄
D₅
D₆
D₇
D₈
D₉
D₁₀
D₁₁
D₁₂
D₁₃
D₁₄
D₁₅
D₁₆
D₁₇
D₁₈
D₁₉
D₂₀
D₂₁
D₂₂
D₂₃
D₂₄
D₂₅
D₂₆
D₂₇
D₂₈
D₂₉
D₃₀
D₃₁


A0
A1
A2
A3
A4
3-8
Decoder
2-4
Decoder
D0
D1
D2
D3
D7
A2'A1'A0'
A2'A1'A0
A4'A4
A3'A2
A4A3
D0
D1
D2
D3
D4
D7
D30
D31
A4'A3'A2'A1'A0'
A4'A3'A2'A1'A0
A4A3A2A1A0