Lecture Notes

Power MOSFETs

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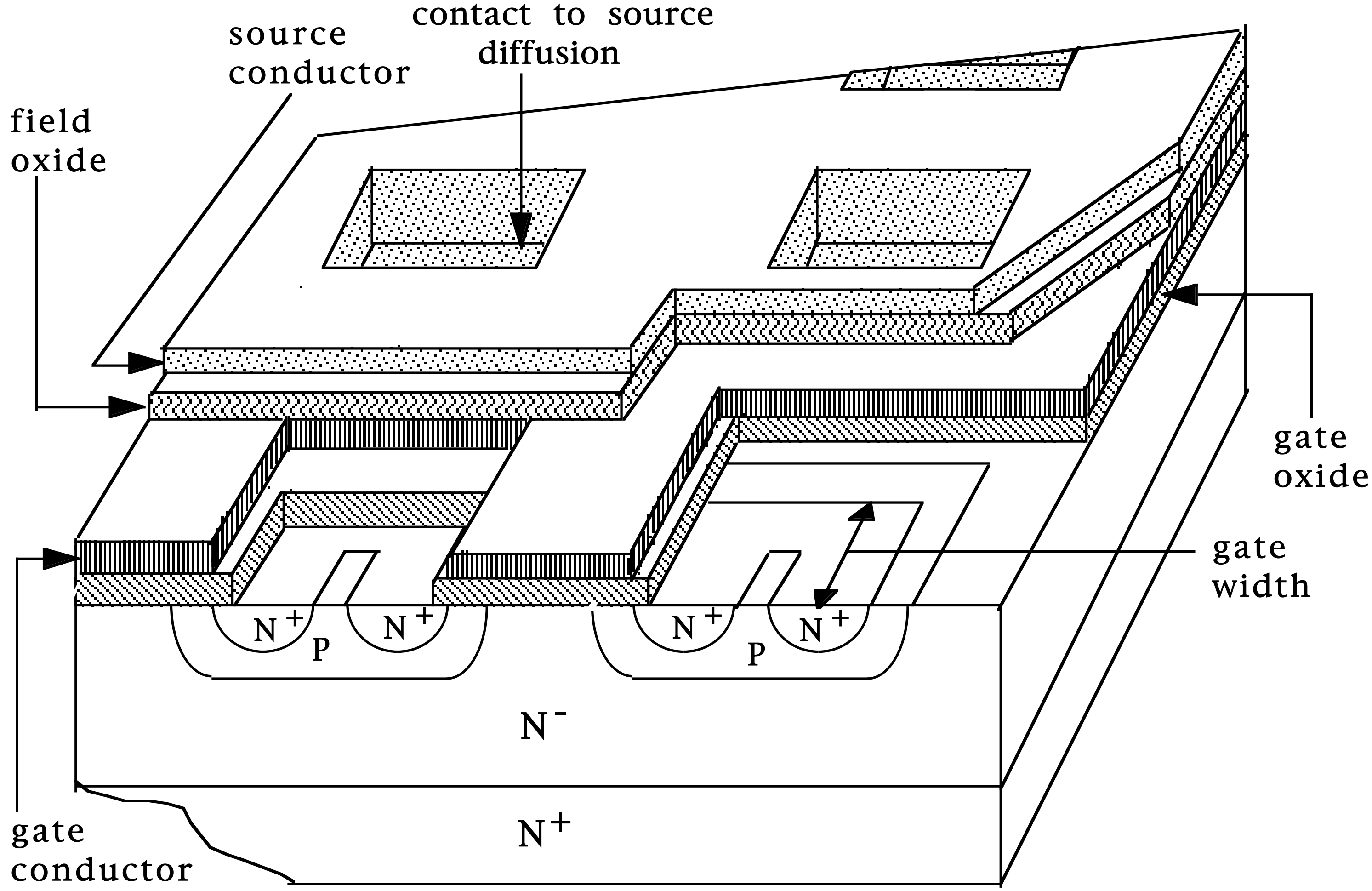
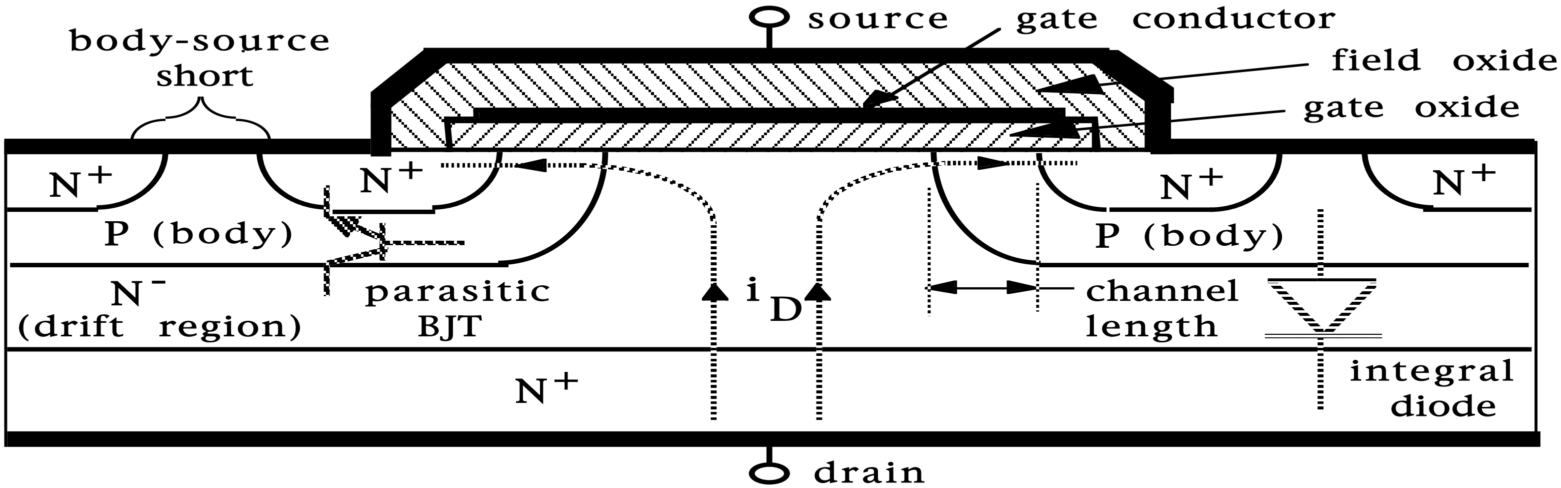
Outline

- Construction of power MOSFETs
- Physical operations of MOSFETs
- Power MOSFET switching Characteristics
- Factors limiting operating specfications of MOSFETs
- COOLMOS
- PSPICE and other simulation models for MOSFETs

Multi-cell Vertical Diffused Power MOSFET (VDMOS)

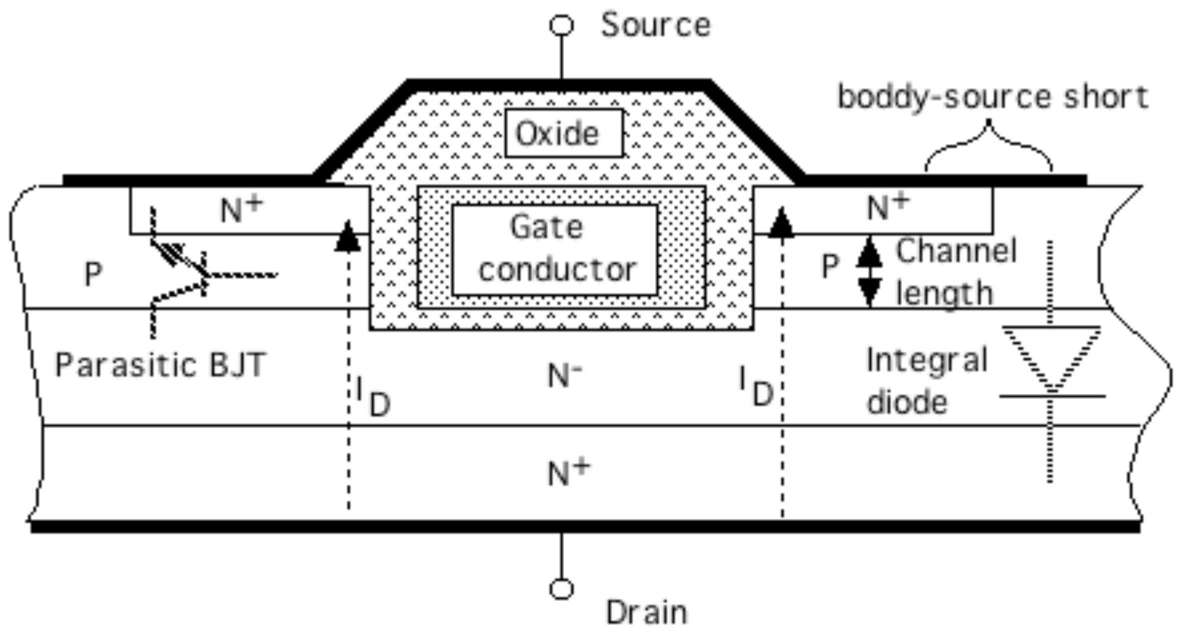


Important Structural Features of VDMOS

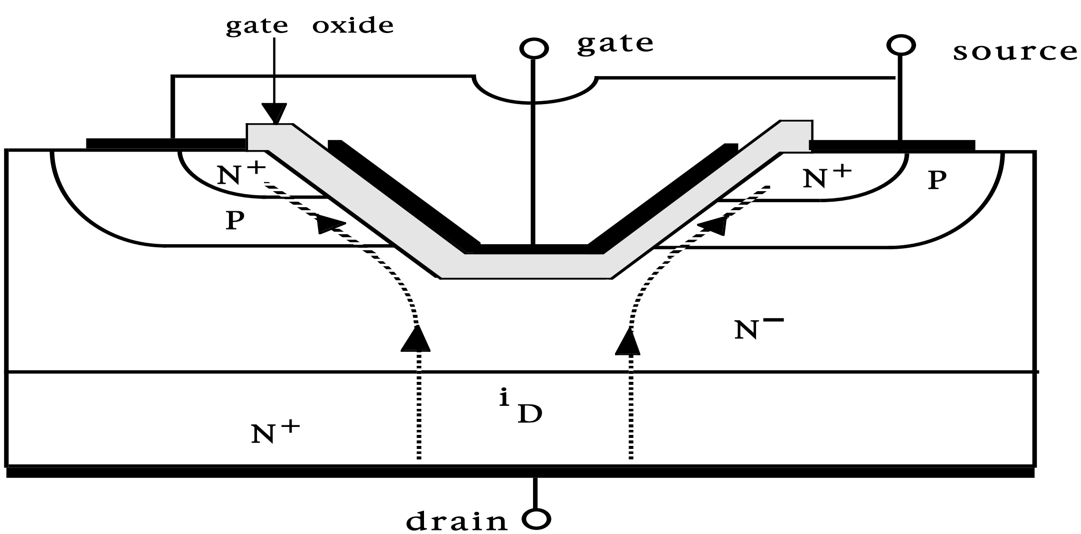


1. Parasitic BJT. Held in cutoff by body-source short
2. Integral anti-parallel diode. Formed from parasitic BJT.
3. Extension of gate metallization over drain drift region. Field plate and accumulation layer functions.
4. Division of source into many small areas connected electrically in parallel. Maximizes gate width-to-channel length ratio in order to increase gain.
5. Lightly doped drain drift region. Determines blocking voltage rating.

Alternative Power MOSFET Geometries

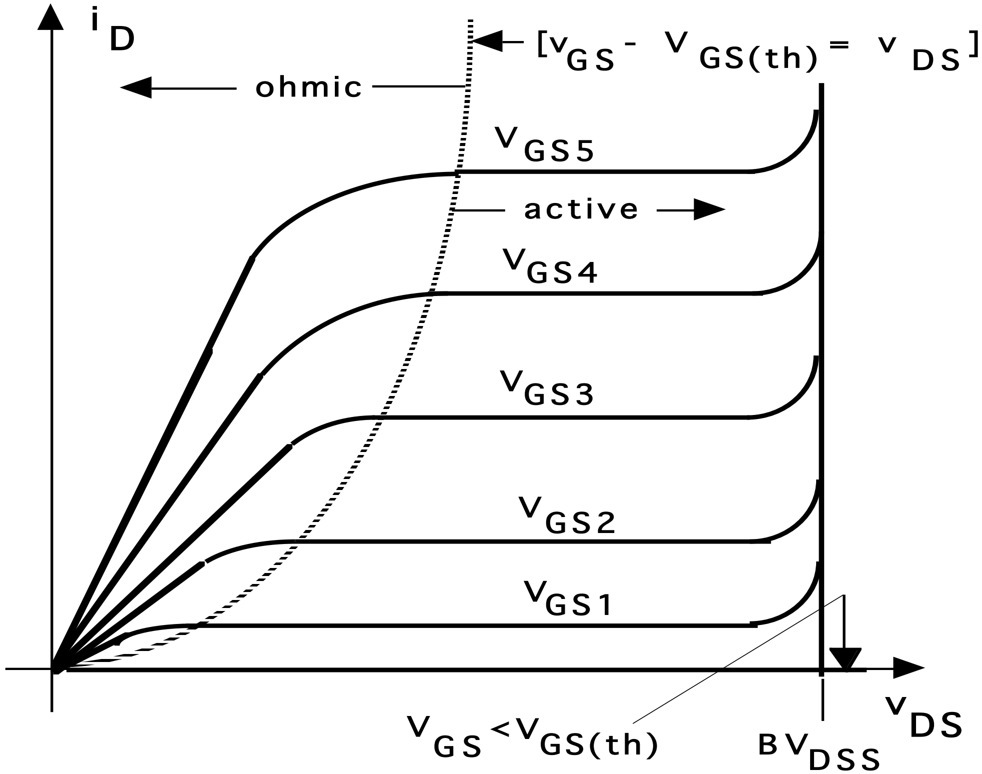


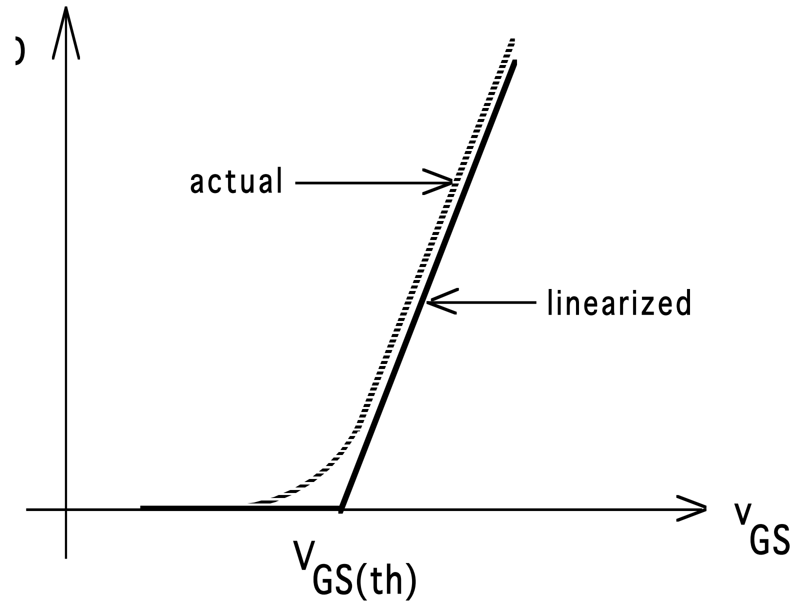
- Trench-gate MOSFET
- Newest geometry. Lowest on-state resistance.

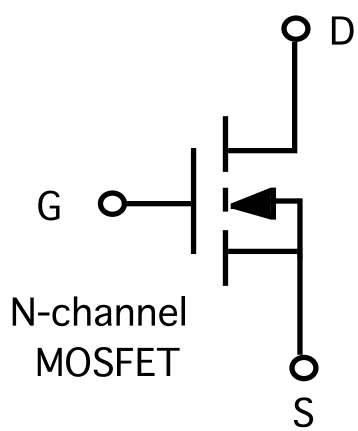


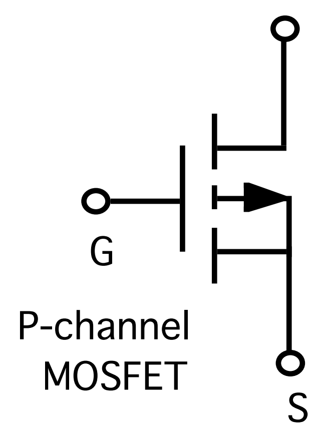
- V-groove MOSFET.
- First practical power MOSFET.
- Higher on-state resistance.

MOSFET I-V Characteristics and Circuit Symbols

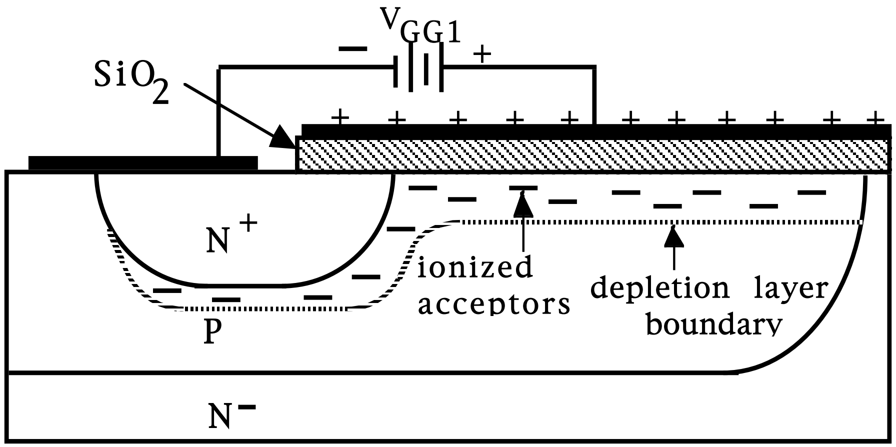


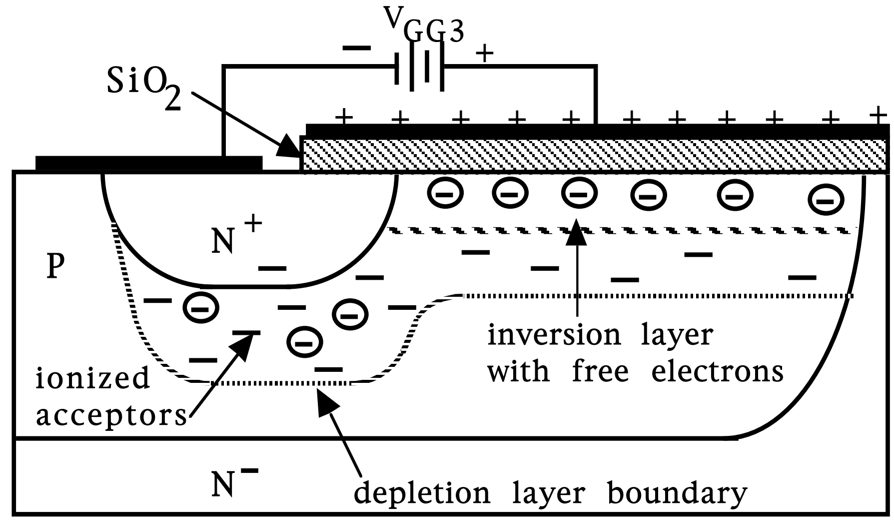


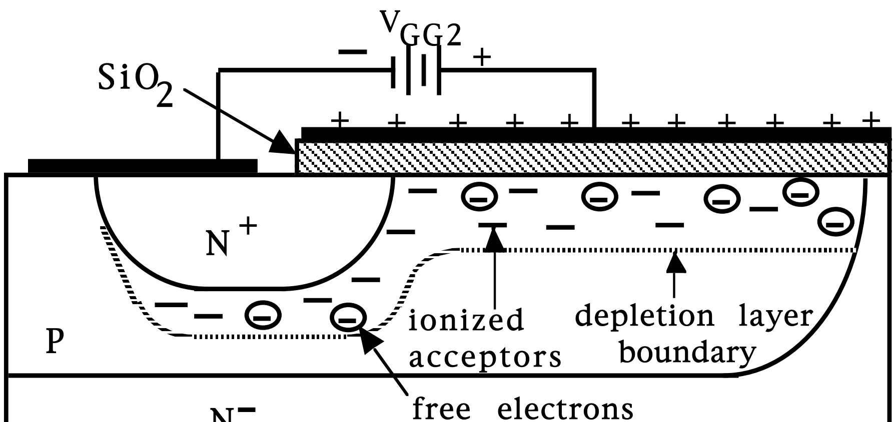




The Field Effect - Basis of MOSFET Operation







Threshold Voltage $V_{GS(th)}$

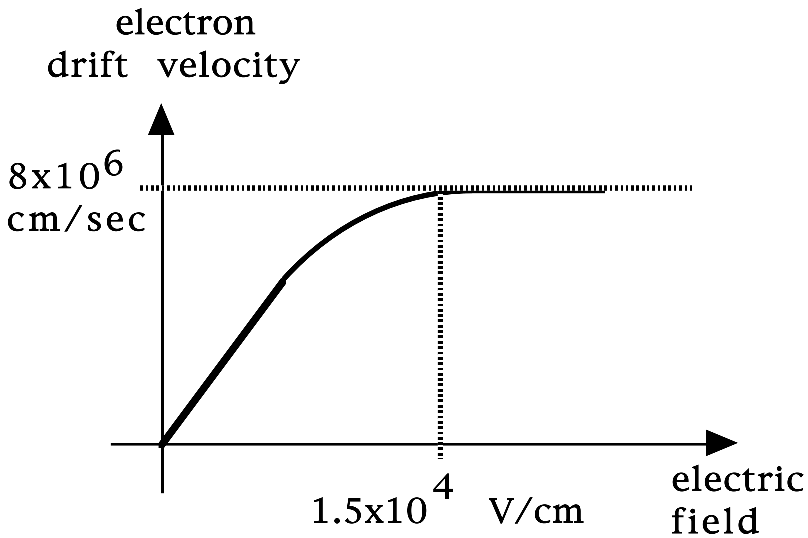
- V_{GS} where strong inversion layer has formed. Typical values 2- 5 volts in power MOSFETs

- Value determined by several factors
  1. Type of material used for gate conductor
  2. Doping density of body region directly beneath gate
  3. Impurities/bound charges in oxide
  4. Oxide capacitance per unit area $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

     t_{ox} = oxide thickness

- Adjust threshold voltage during device fabrication via an ion implantation of impurities into body region just beneath gate oxide.

Drift Velocity Saturation



- In MOSFET channel, $J = q\ \mu_n\ n\ E$ $= q\ n\ v_n$; velocity $v_n = \mu_n\ E$

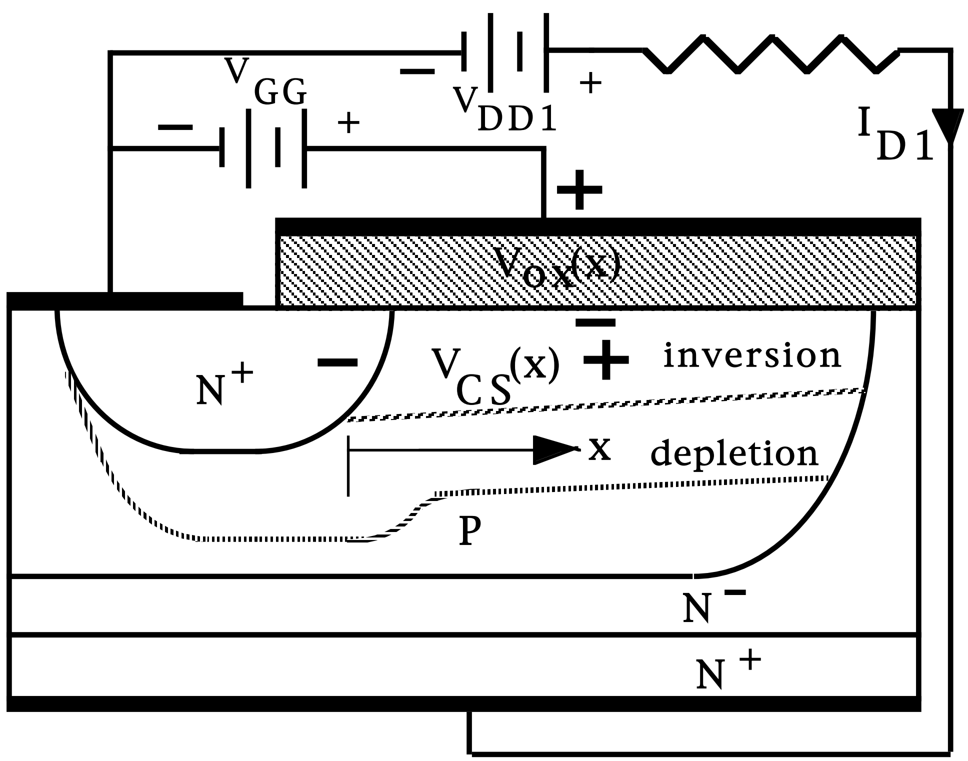
- Velocity saturation means that the mobility μ_n inversely proportional to electric field E.

- Mobility also decreases because large values of V_{GS} increase free electron density.

- At larger carrier densities, free carriers collide with each other (carrier-carrier scattering) more often than with lattice and mobility decreases as a result.

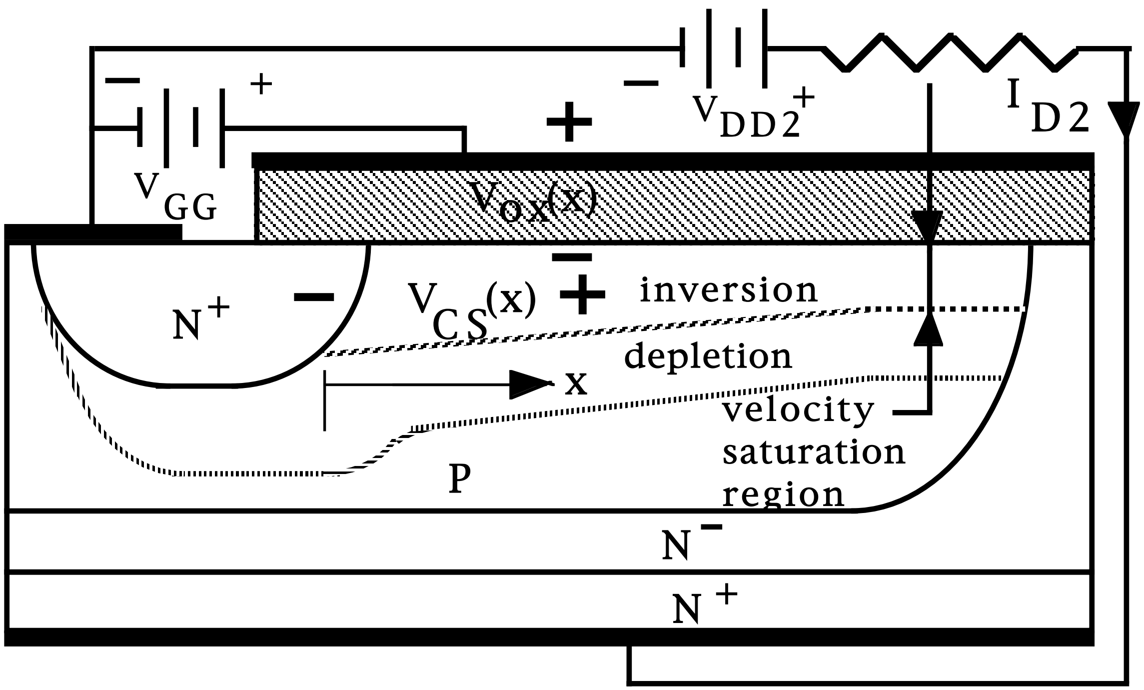
- Mobilty decreases, especially via carrier-carrier scattering leead to linear transfer curve in power devices instead of square law transfer curve of logic level MOSFETs.

Channel-to-Source Voltage Drop



- $V_{GS} = V_{GG} = V_{ox} + V_{CS}(x)$; $V_{CS}(x) = I_{D1} R_{CS}(x)$
- Larger x value corresponds be being closer to the drain and to a smaller V_{ox}.
- Smaller V_{ox} corresponds to a smaller channel thickness. Hence reduction in channel thickness as drain is approached from the source.

Channel Pinch-off at Large Drain Current



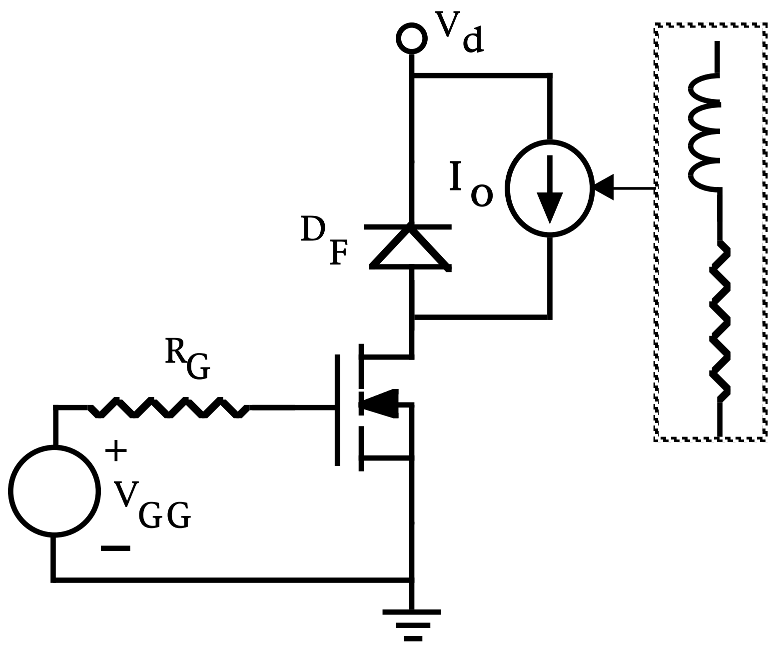
- $I_{D2} > I_{D1}$ so $V_{CS2}(x) > V_{CS1}(x)$ and thus channel narrower at an given point.
- Total channel resistance from drain to source increasing and curve of I_D vs V_{DS} for a fixed V_{GS} flattens out.

- Apparent dilemma of channel disappearing at drain end for large I_D avoided.

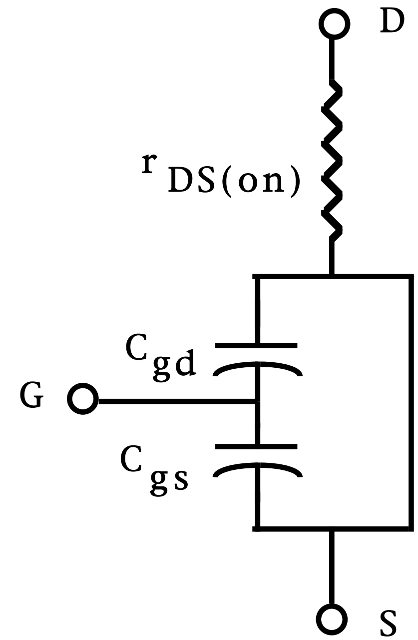
1. Large electric field at drain end oriented parallel to drain current flow. Arises from large current flow in channel constriction at drain.
2. This electric field takes over maintenance of minimum inversion layer thickness at drain end.

- Larger gate-source bias V_{GG} postpones flattening of I_D vs V_{DS} until larger values of drain current are reached.

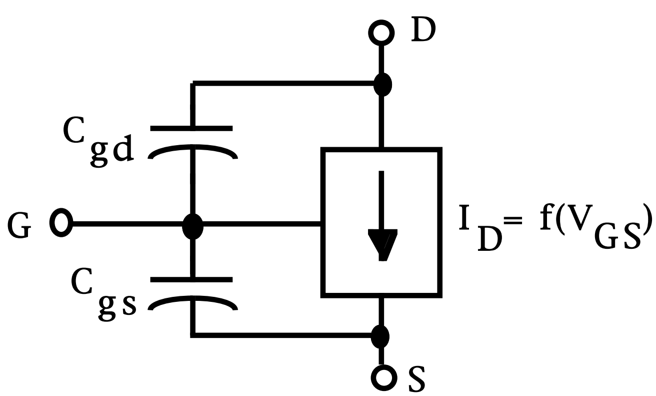
MOSFET Switching Models for Buck Converter



• Buck converter using power MOSFET.

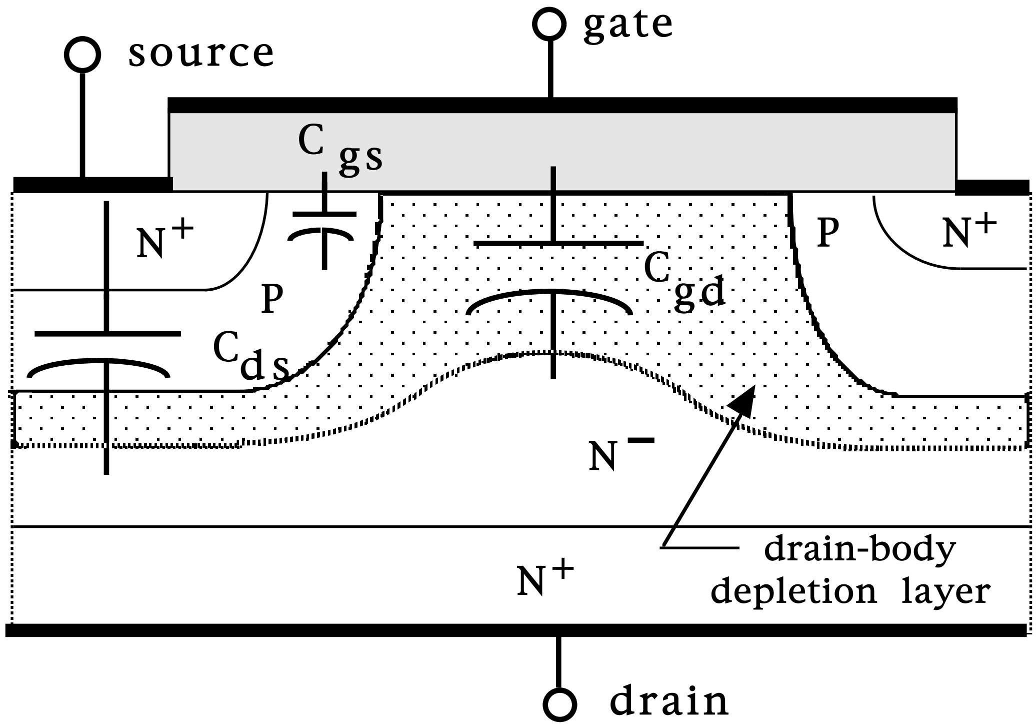


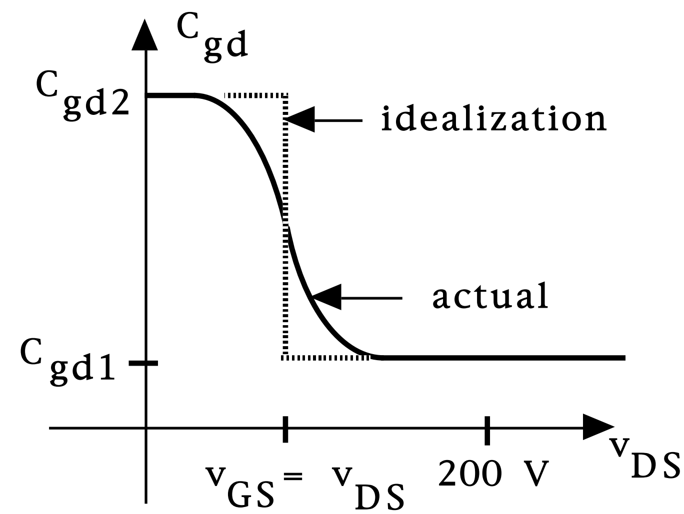
• MOSFET equivalent circuit valid for on-state (triode) region operation.



• MOSFET equivalent circuit valid for off - state (cutoff) and active region operation.

MOSFET Capacitances Determining Switching Speed

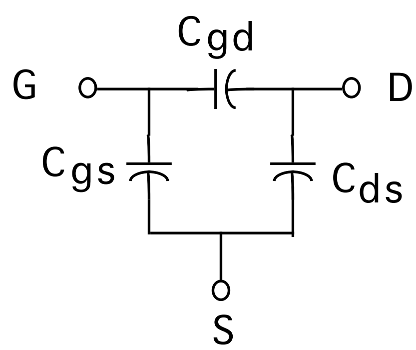




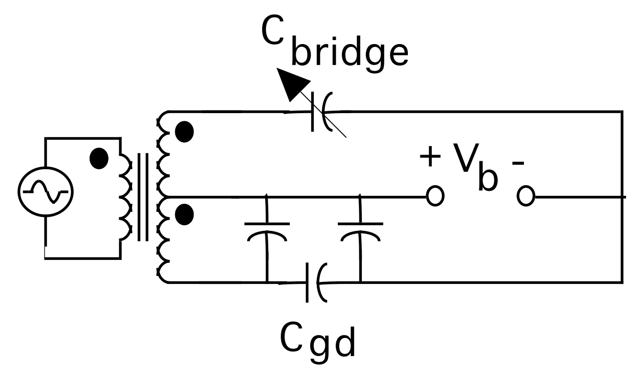
- Gate-source capacitance Cgs approximately constant and independent of applied voltages.
- Gate-drain capacitance C_{gd} varies with applied voltage. Variation due to growth of depletion layer thickness until inversion layer is formed.

Internal Capacitances Vs Spec Sheet Capacitances

MOSFET internal capacitances

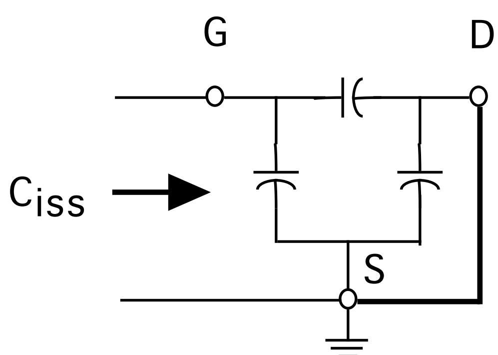


Reverse transfer or feedback capacitance



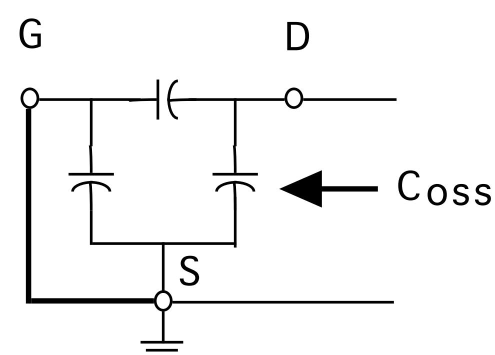
Bridge balanced (Vb=0) Cbridge = Cgd $= C_{rss}$

Input capacitance



$C_{iss} = C_{gs} + C_{gd}$

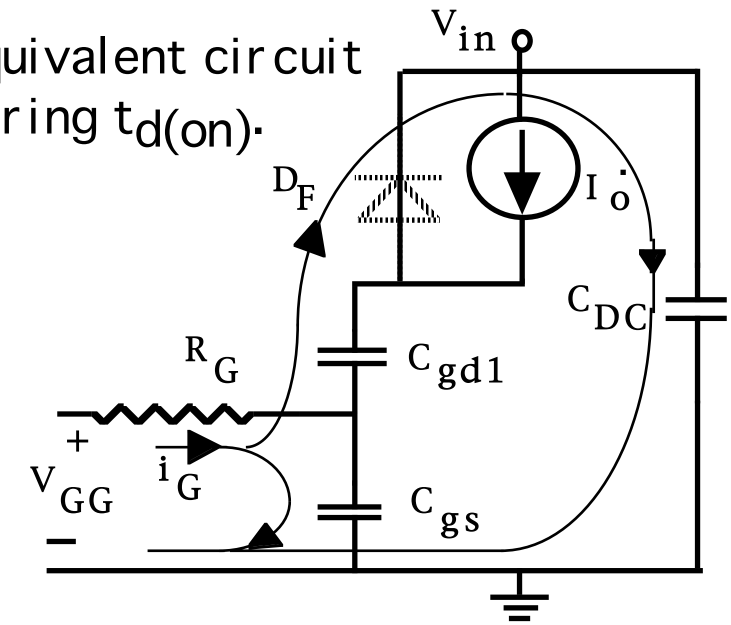
Output capacitance



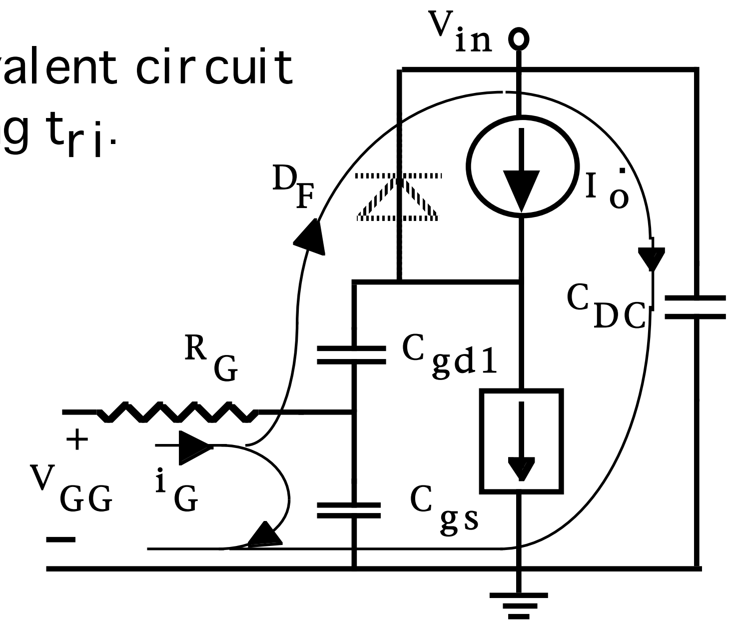
$C_{oss} = C_{gd} + C_{ds}$

Turn-on Equivalent Circuits for MOSFET Buck Converter

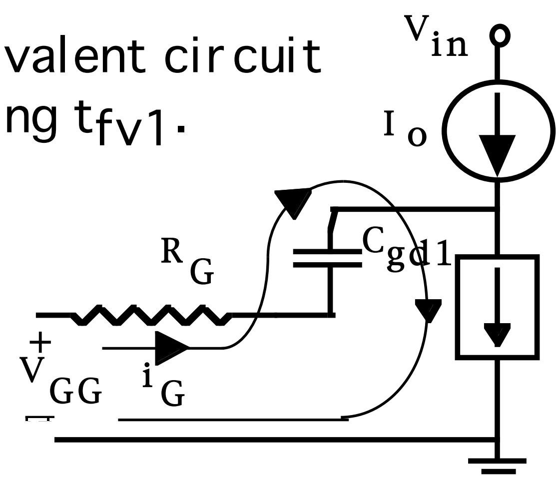
- Equivalent circuit during $t_{d(on)}$.



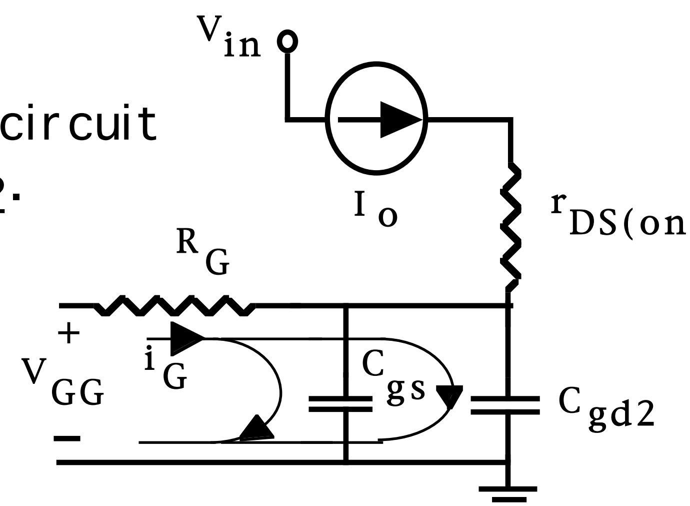
- Equivalent circuit during t_{ri}.



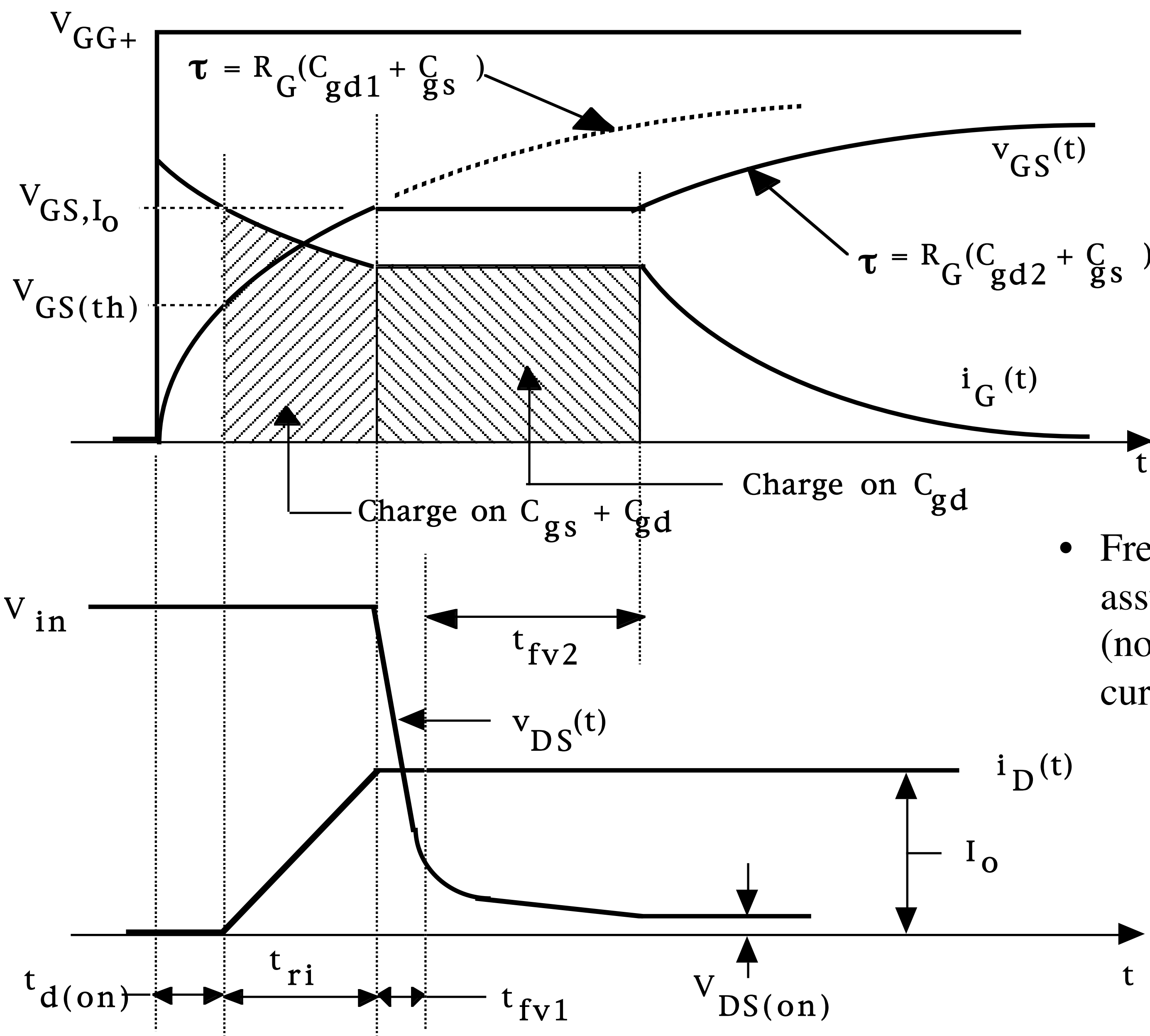
- Equivalent circuit during t_{fv1}.



- Equivalent circuit during t_{fv2}.

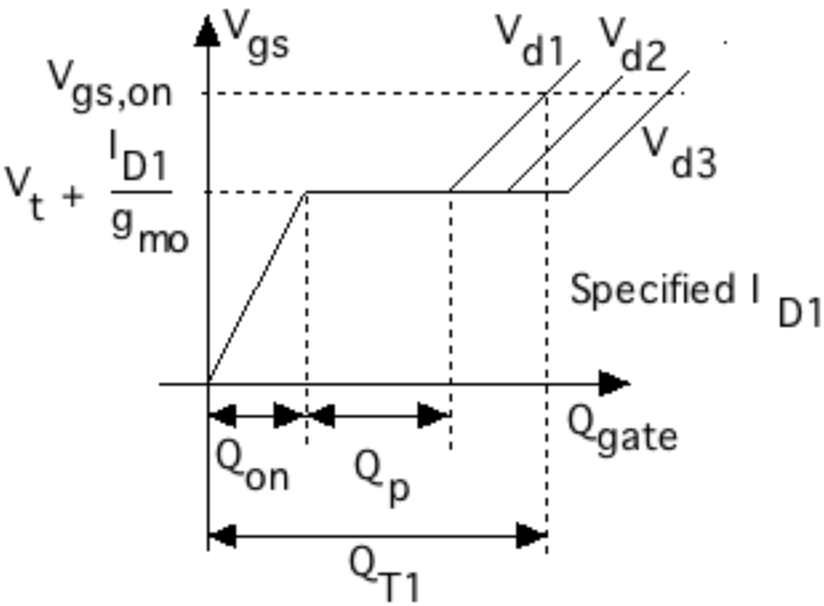


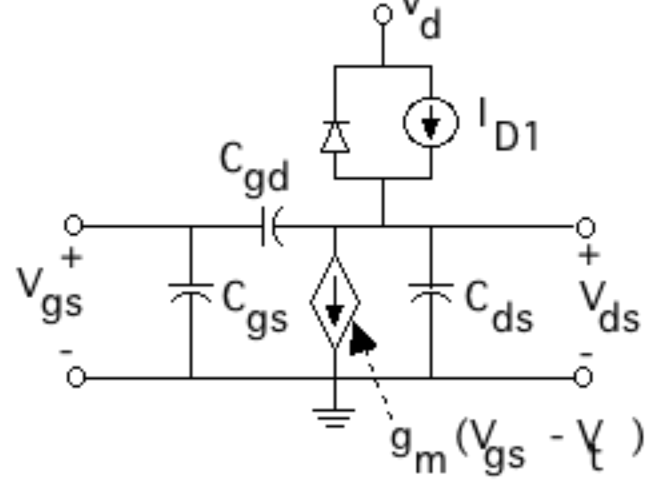
MOSFET-based Buck Converter Turn-on Waveforms

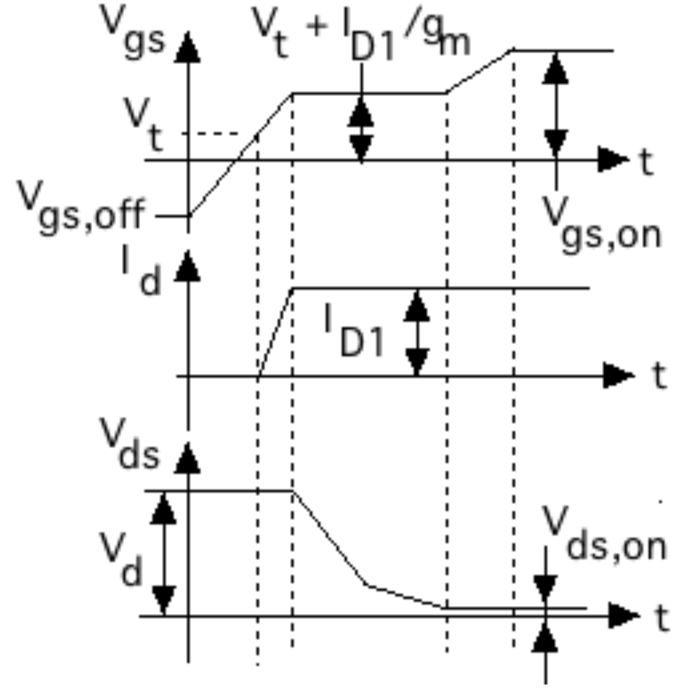


- Free-wheeling diode assumed to be ideal. (no reverse recovery current).

Turn-on Gate Charge Characteristic





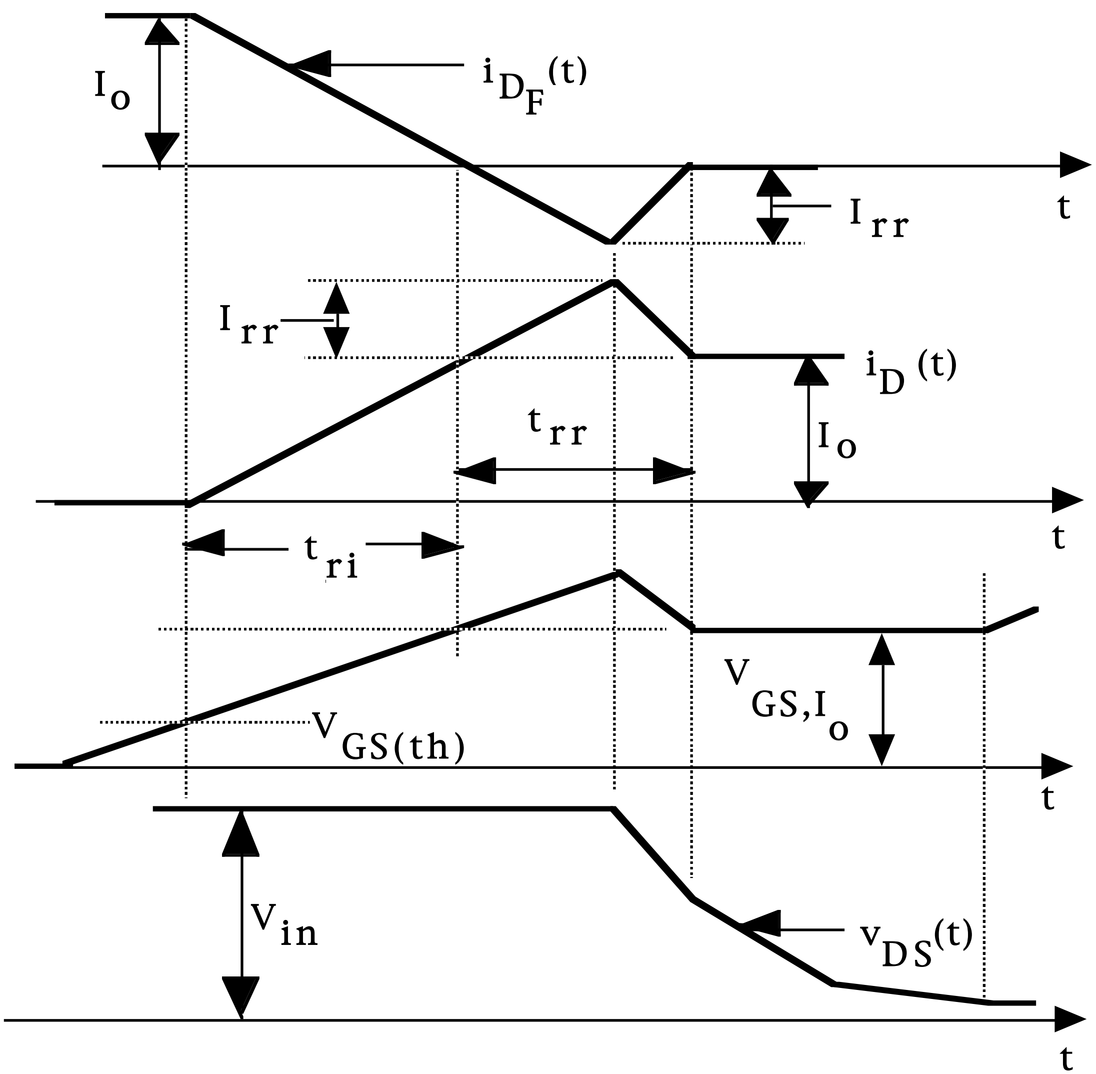


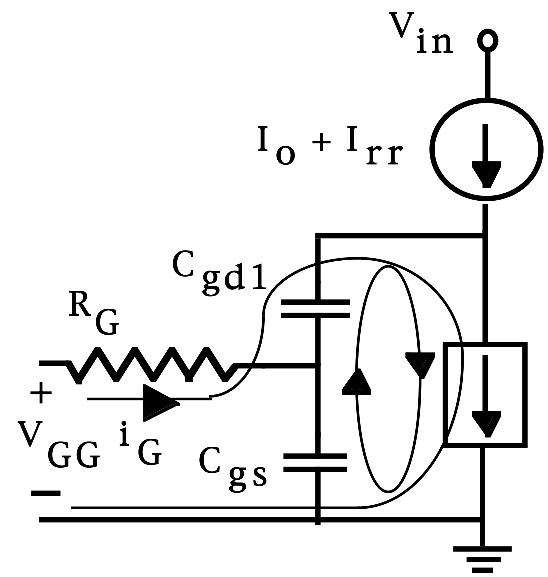
$$Q_{on} = \int_{V_{gs,off}}^{(V_t + I_{D1}/g_m)} [C_{gs}(V_{gs}) + C_{gd}(V_{gs})]\, V_{gs}\, dV_{gs}$$

$$Q_p = \int_{V_d}^{V_{ds,on}} C_{gd}(V_{ds})\, V_{ds}\, dV_{ds}$$

$$Q_T = Q_{on} + Q_p + \int_{(V_t + I_{D1}/g_m)}^{V_{gs,on}} [C_{gs}(V_{gs}) + C_{gd}(V_{gs})]\, V_{gs}\, dV_{gs}$$

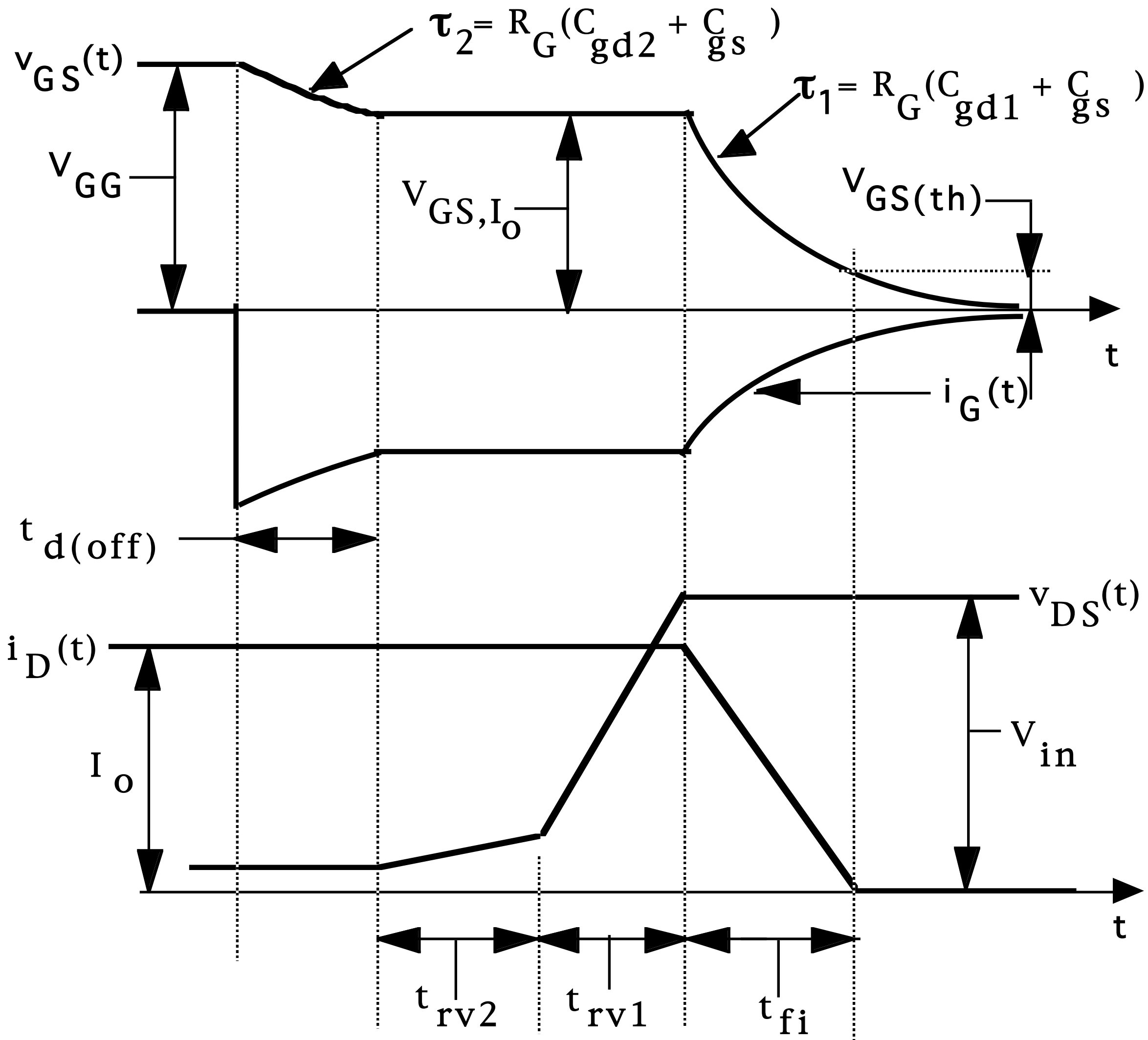
Turn-on Waveforms with Non-ideal Free-wheeling Diode





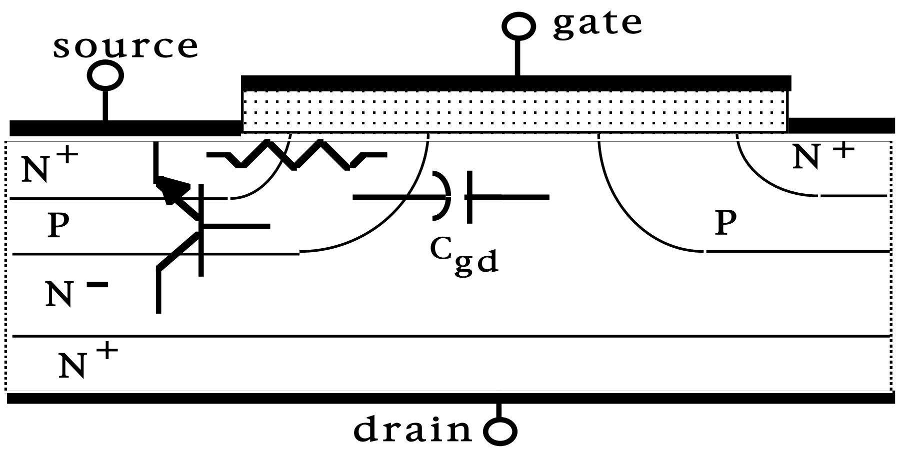
- Equivalent circuit for estimating effect of free -wheeling diode reverse recovery.

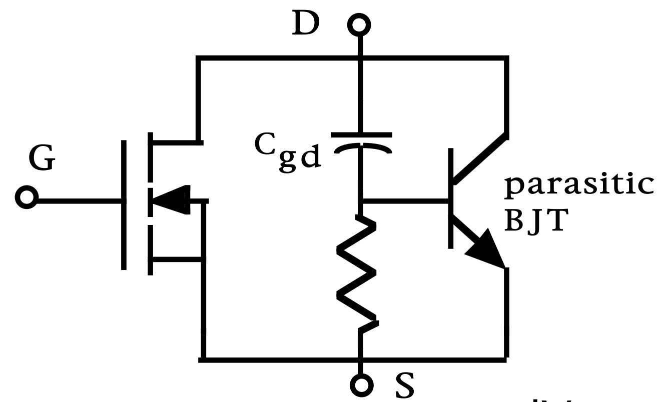
MOSFET-based Buck Converter Turn-off Waveforms



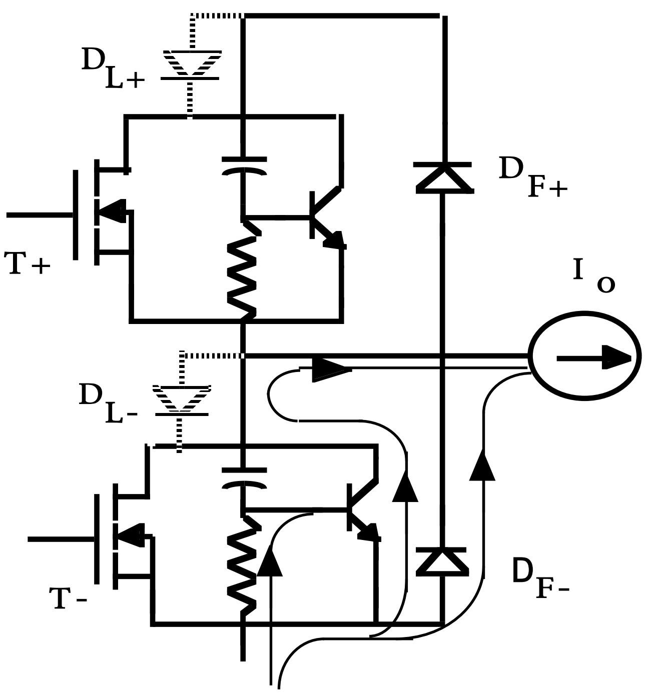
- Assume ideal free-wheeling diode.
- Essentially the inverse of the turn-on process.
- Model quanitatively using the same equivalent circuits as for turn-on. Simply use correct driving voltages and initial conditions

dV/dt Limits to Prevent Parasitic BJT Turn-on





- Large positive $C_{gd} \frac{dV_{DS}}{dt}$ could turn on parasitic BJT.



- Turn-on of T_+ and reverse recovery of D_{f-} will produce large positive $C_{gd} \frac{dv_{DS}}{dt}$ in bridge circuit.
- Parasitic BJT in T_- likely to have been in reverse active mode when D_{f-} was carrying current. Thus stored charge already in base which will increase likeyhood of BJT turn-on when positive $C_{gd} \frac{dv_{DS}}{dt}$ is generated.

Maximum Gate-Source Voltage

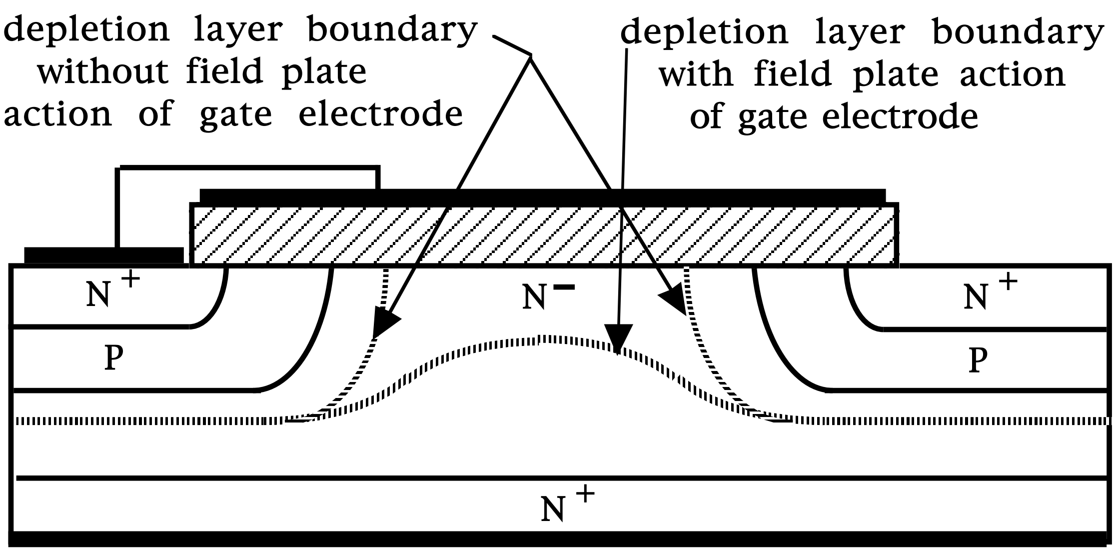
- $V_{GS(max)}$ = maximum permissible gate-source voltage.

- If $V_{GS} > V_{GS(max)}$ rupture of gate oxide by large electric fields possible.

- E_{BD}(oxide) ≈ 5-10 million V/cm
  - Gate oxide typically 1000 anstroms thick
  - $V_{GS(max)} < [5x10^6] [10^{-5}] = 50$ V
  - Typical $V_{GS(max)}$ 20 - 30 V

- Static charge on gate conductor can rupture gate oxide
  - Handle MOSFETs with care (ground yourself before handling device)
  - Place anti-parallel connected Zener diodes between gate and source as a protective measure

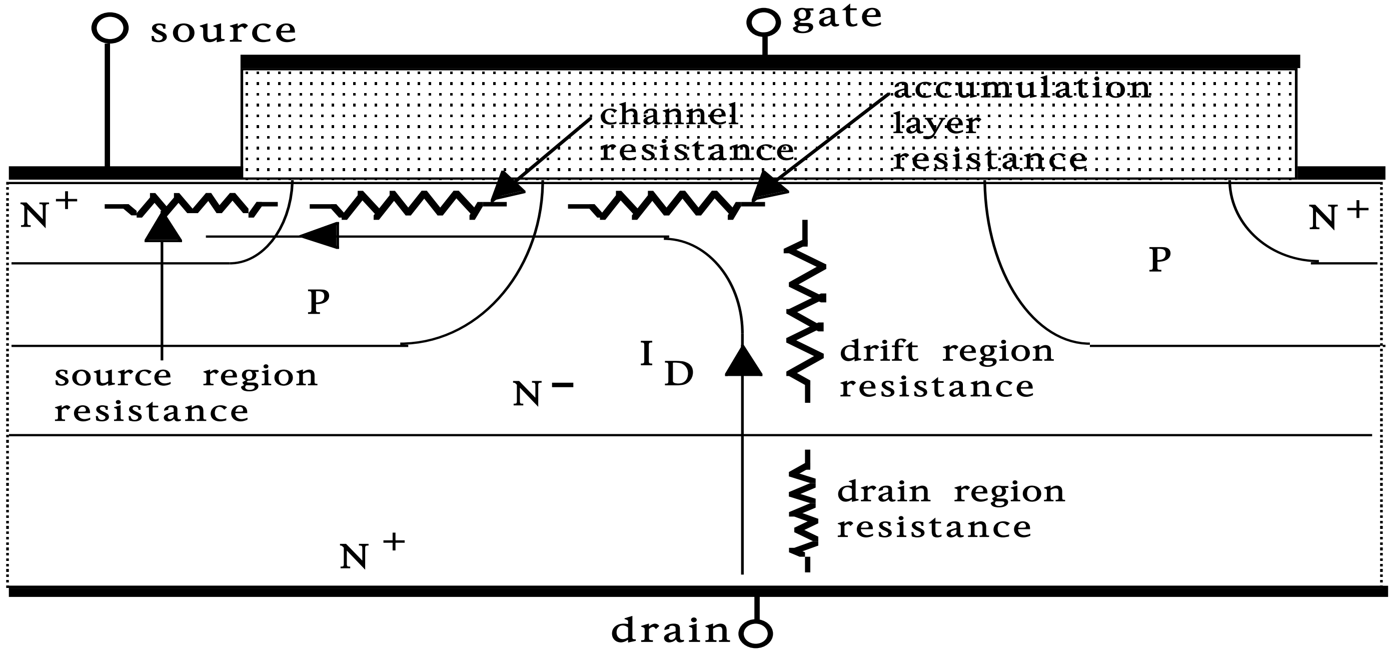
MOSFET Breakdown Voltage



- BV_{DSS} = drain-source breakdown voltage with V_{GS} = 0
- Caused by avalanche breakdown of drain-body junction
- Achieve large values by

  1. Avoidance of drain-source reach-through by heavy doping of body and light doping of drain drift region
  2. Appropriate length of drain drift region
  3. Field plate action of gate conductor overlap of drain region
  4. Prevent turn-on of parasitic BJT with body-source short (otherwise BV_{DSS} = BV_{CEO} instead of BV_{CBO})

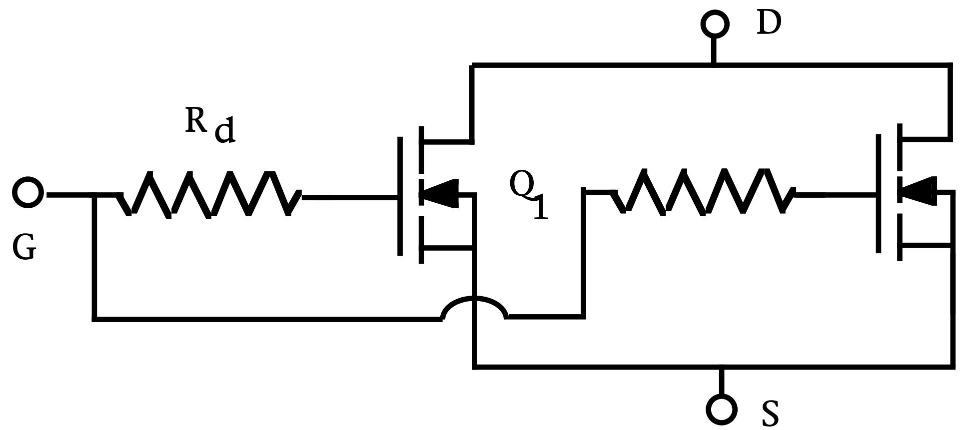
MOSFET On-state Losses



- On-state power dissipation $P_{on} = I_o^2 \, r_{DS(on)}$
- Large V_{GS} minimizes accumulation layer resistance and channel resistance
- $r_{DS(on)}$ dominated by drain drift resistance for BV_{DSS} > few 100 V
- $r_{DS(on)} = \frac{V_d}{I_D} \approx 3 \times 10^{-7} \frac{BV_{DSS}^2}{A}$
- $r_{DS(on)}$ increases as temperature increases. Due to decrease in carrier mobility with increasing temperature.

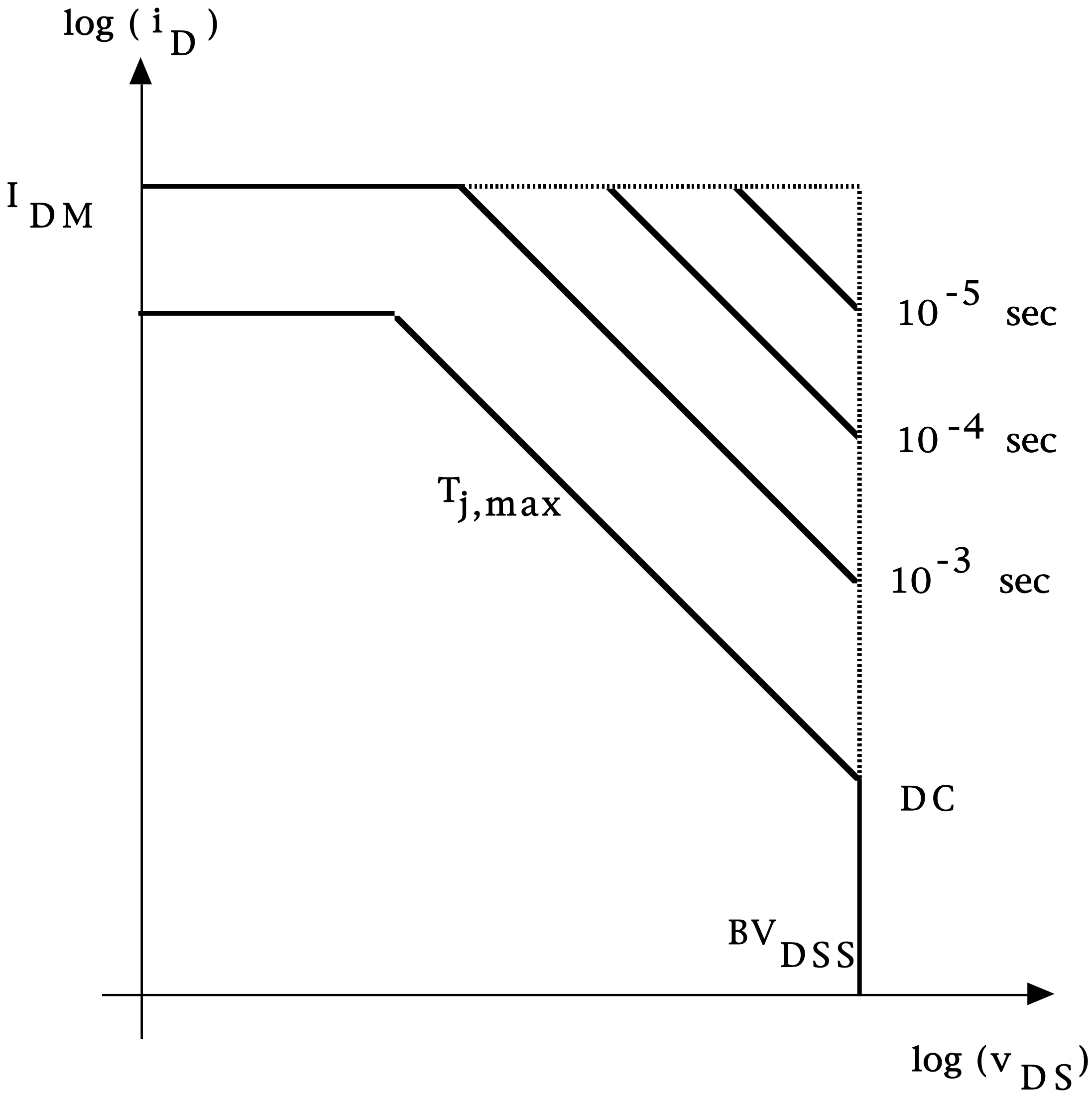
Paralleling of MOSFETs

- MOSFETs can be easily paralleled because of positive temperature coefficient of $r_{DS(on)}$.



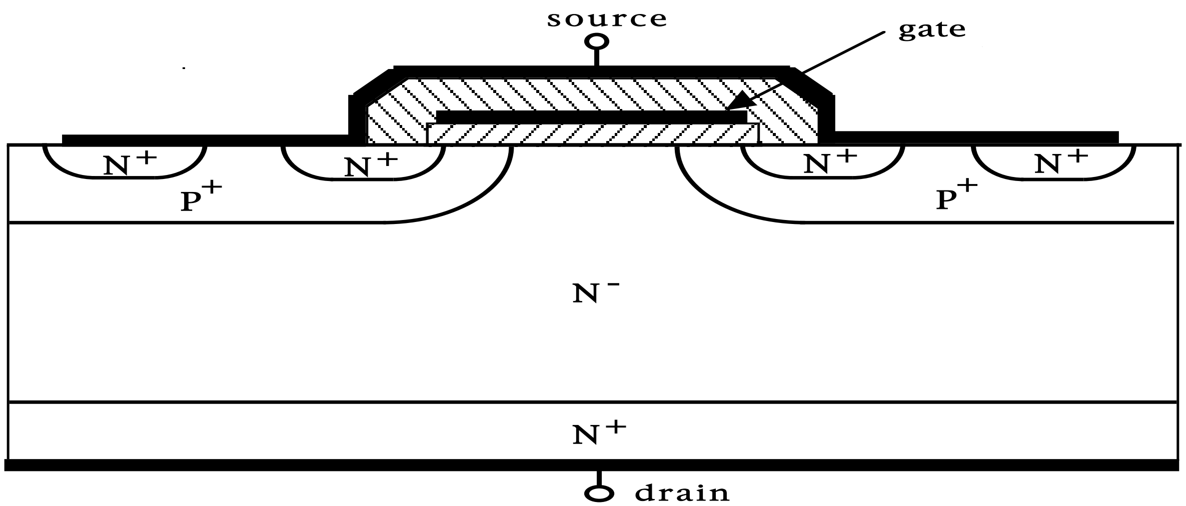
- Positive temperature coefficient leads to thermal stabilization effect.
  - If $r_{DS(on)1} > r_{DS(on)2}$ then more current and thus higher power dissipation in Q_2.
  - Temperature of Q_2 thus increases more than temperature of Q_1 and $r_{DS(on)}$ values become equalized.

MOSFET Safe Operating Area (SOA)

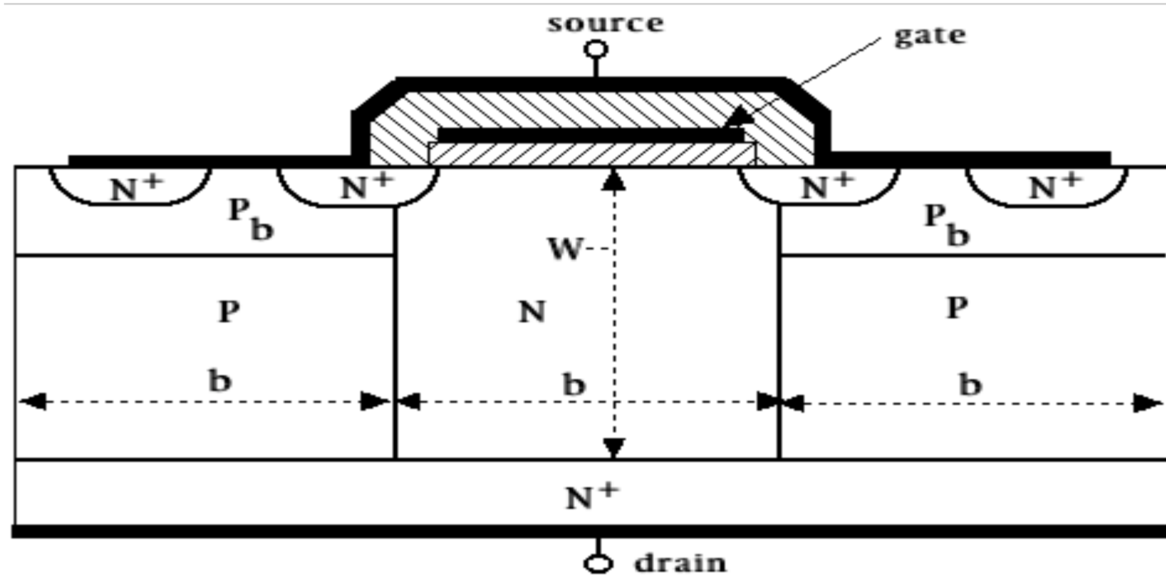


- No distinction between FBSOA and RBSOA. SOA is square.
  - FB = forward bias. $V_{GS} \geq 0$.
  - RB = reverse bias. $V_{GS} \leq 0$.
- No second breakdown.

Structural Comparison: VDMOS Versus COOLMOS™

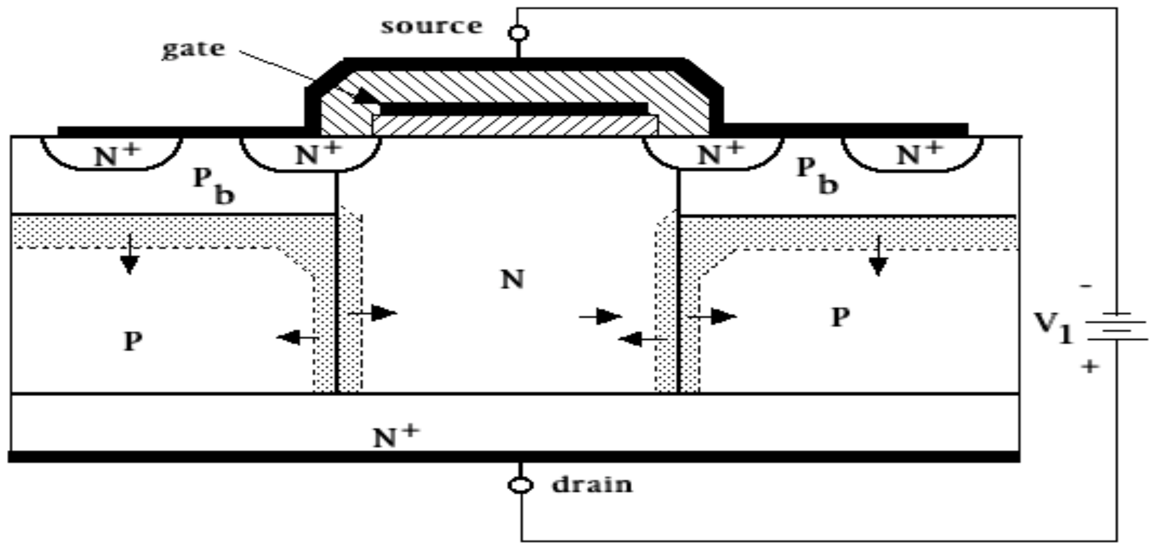


- Conventional vertically oriented power MOSFET

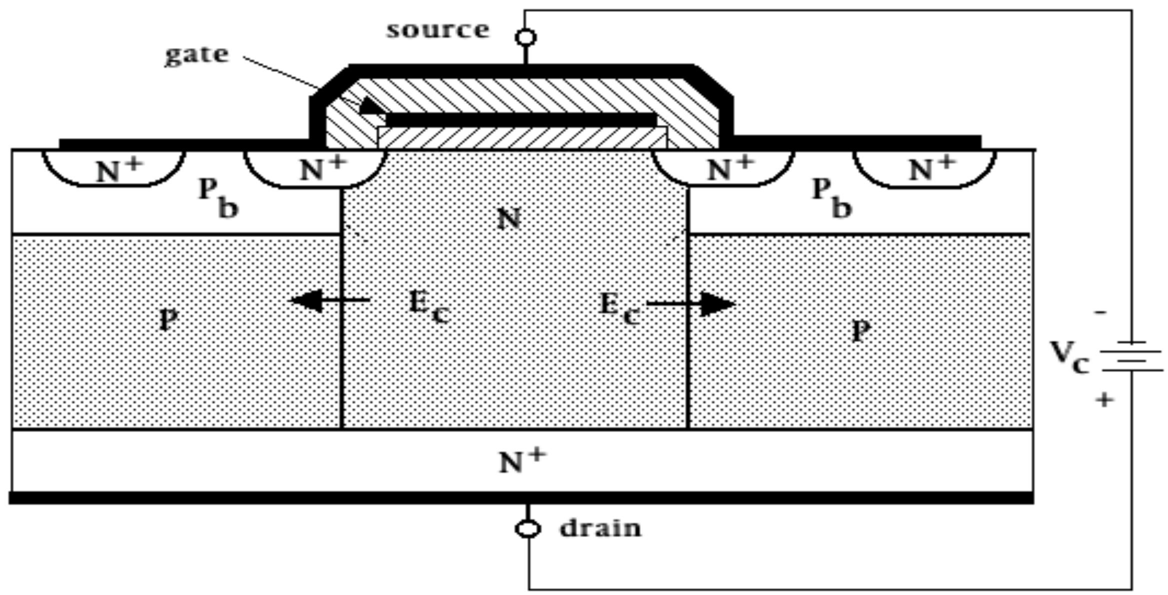


- COOLMOS™ structure (composite buffer structure, super-junction MOSFET, super multi -resurf MOSFET)
- Vertical P and N regions of width b doped at same density ($N_a = N_d$)

COOLMOS™ Operation in Blocking State

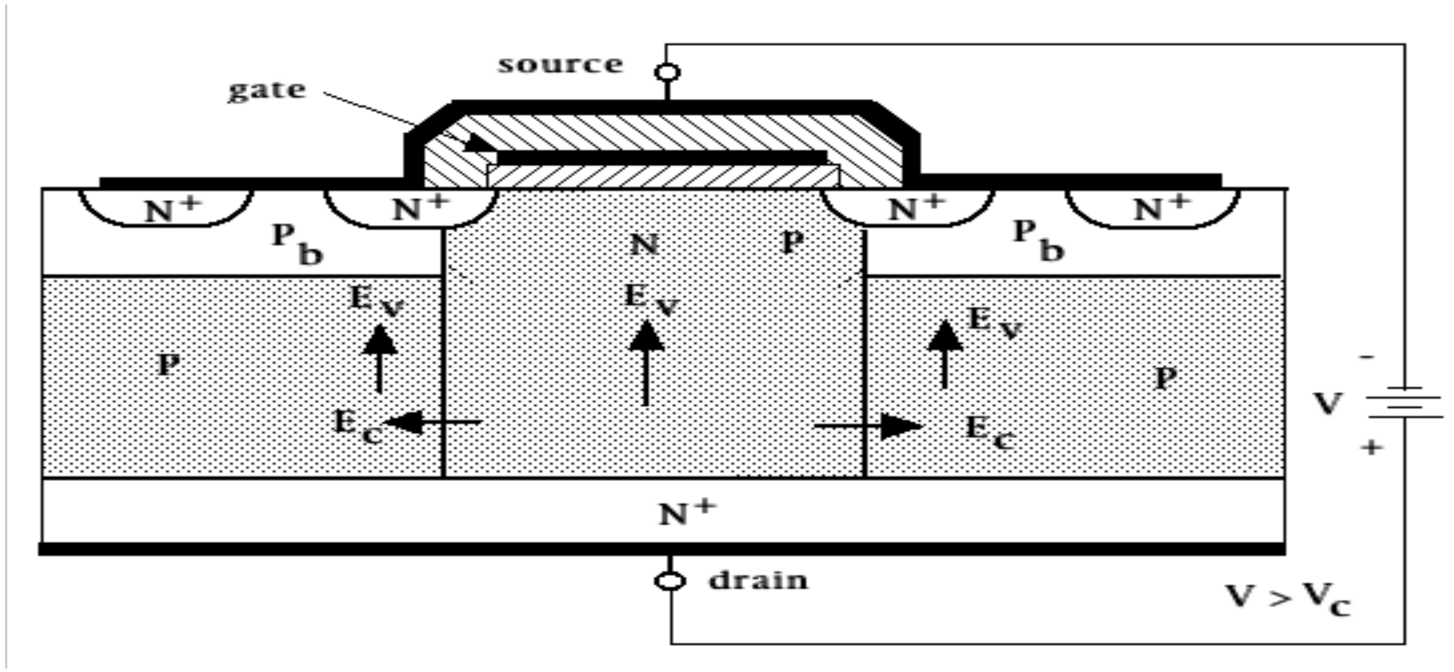


- COOLMOS™ structure partially depleted.
- Arrows indicate direction of depletion layer growth as device turns off.
- Note n-type drift region and adjacent p-type stripes deplete uniformly along entire vertical length.



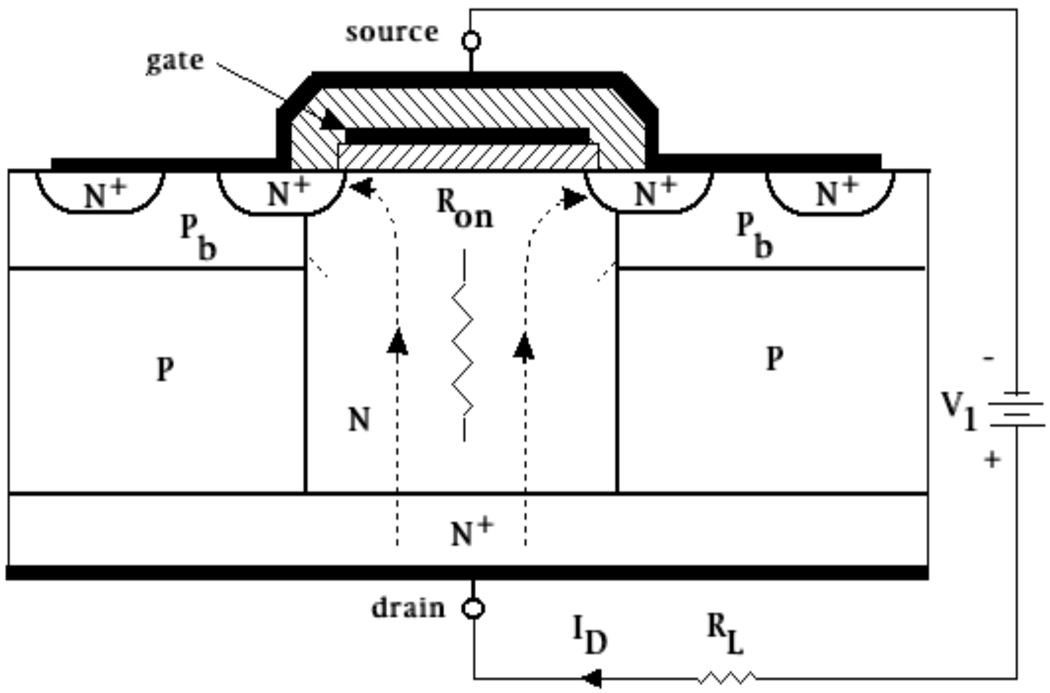
- COOLMOS™ structure at edge of full depletion with applied voltage V_c. Depletion layer reaches to middle of vertical P and N regions at b/2.
- Using step junction formalism, $V_c = (q\, b^2\, N_d)/(4\, \varepsilon) = b\, E_{c,max}/2$
- Keep $E_{c,max} \leq E_{BD}/2$. Thus $N_d \leq (\varepsilon\, E_{BD})/(q\, b)$

COOLMOS™ Operation in Blocking State (cont.)



- For applied voltages $V > V_c$, vertically oriented electric field E_v begins to grow in depletion region.
- E_v spatially uniform since space charge compensated for by E_c. $E_v \approx V/W$ for $V >> V_c$.
- Doping level N_d in n-type drift region can be much greater than in drift region of conventional VDMOS drift region of similar BV_{BD} capability.
- At breakdown $E_v = E_{BD} \approx 300$ kV/cm ; $V = BV_{BD} = E_{BD}W$

COOLMOS™ Operation in ON-State



- On-state specific resistance AR_{on} [Ω-cm[2]] much less than comparable VDMOS because of higher drift region doping.
- COOLMOS™ conduction losses much less than comparable VDMOS.

- $R_{on} A = W/(q\, \mu_n N_d)$; Recall that $N_d = (\varepsilon\, E_{BD})/(q\, b)$
- Breakdown voltage requirements set $W = BV_{BD}/ E_{BD}$.
- Substituting for W and N_d yields $R_{on} A = (b\, BV_{BD})/(\varepsilon\, \mu_n E_{BD}^2)$

R_{on} A Comparison: VDMOS versus COOLMOS™

- COOLMOS at BV_{BD} = 1000 V. Assume b ≈ 10 μm. Use E_{BD} = 300 kV/cm.
  - R_{on} A = (10^{-3} cm) (1000 V)/[(9×10^{-14} F/cm)(12)(1500 cm^2 -V-sec)(300 kV/cm)^2]

    R_{on} A = 0.014 Ω-cm . Corresponds to $N_d = 4 \times 10^{15}$ cm^{-3}

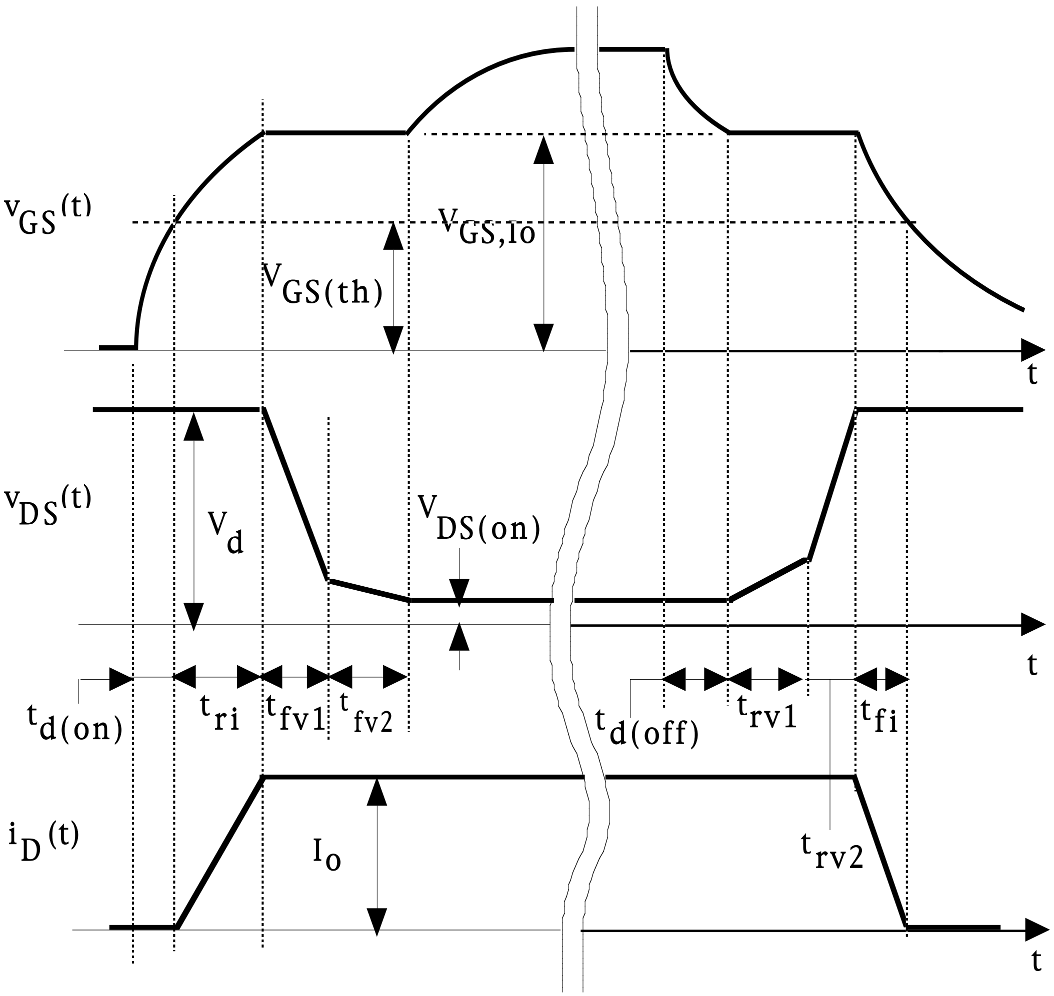
- Typical VDMOS, R_{on} A = 3×10^{-7} $(BV_{BD})^2$
  - R_{on} A = 3×10^{-7} $(1000)^2$ = 0.3 Ω-cm ; Corresponding $N_d = 10^{14}$ cm^3

- Ratio COOLMOS to VDMOS specific resistance = 0.007/0.3 = 0.023 or approximately 1/40
  - At BV_{BD} = 600 V, ratio = 1/26.
  - Experimentally at BV_{BD} = 600 V, ratio is 1/5.

- For more complete analysis see: Antonio G.M. Strollo and Ettore Napoli, “Optimal ON-Resistance Versus Breakdown Voltage Tradeoff in Superjunction Power Device: A Novel Analytical Model”, IEEE Trans. On Electron Devices,Vol. 48, No. 9, pp 2161-2167, (Sept., 2001)

COOLMOS™ Switching Behavior

- MOSFET witching waveforms for clamped inductive load.

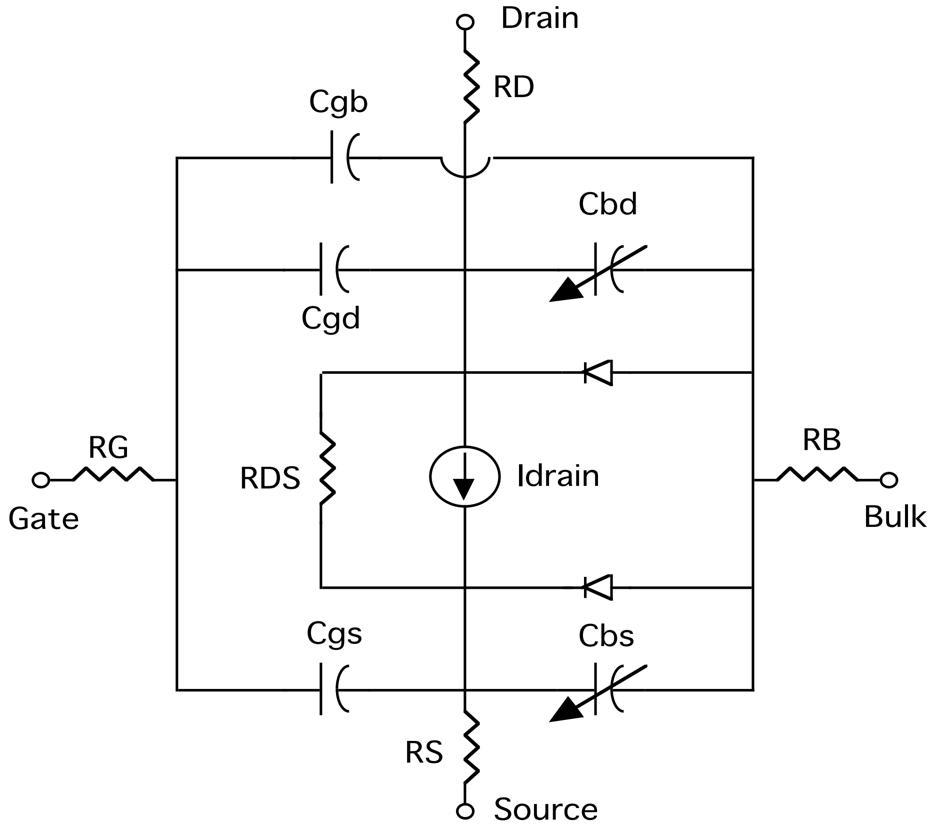


- Larger blocking voltages V_{ds} > depletion voltage V_c, COOLMOS has smaller C_{gs}, C_{gd}, and C_{ds} than comparable (same R_{on} and BV_{DSS}) VDMOS.

- Small blocking voltages V_{ds} < depletion voltage V_c, COOLMOS has larger C_{gs}, C_{gd}, and C_{ds} than comparable (same R_{on} and BV_{DSS}) VDMOS.

- Effect on COOLMOS switching times relative to VDMOS switching times.
  - Turn-on delay time - shorter
  - Current rise time - shorter
  - Voltage fall time1 - shorter
  - Voltage fall time2 - longer
  - Turn-off delay time - longer
  - Voltage rise time1 - longer
  - Voltage rise time2 - shorter
  - Current fall time - shorter

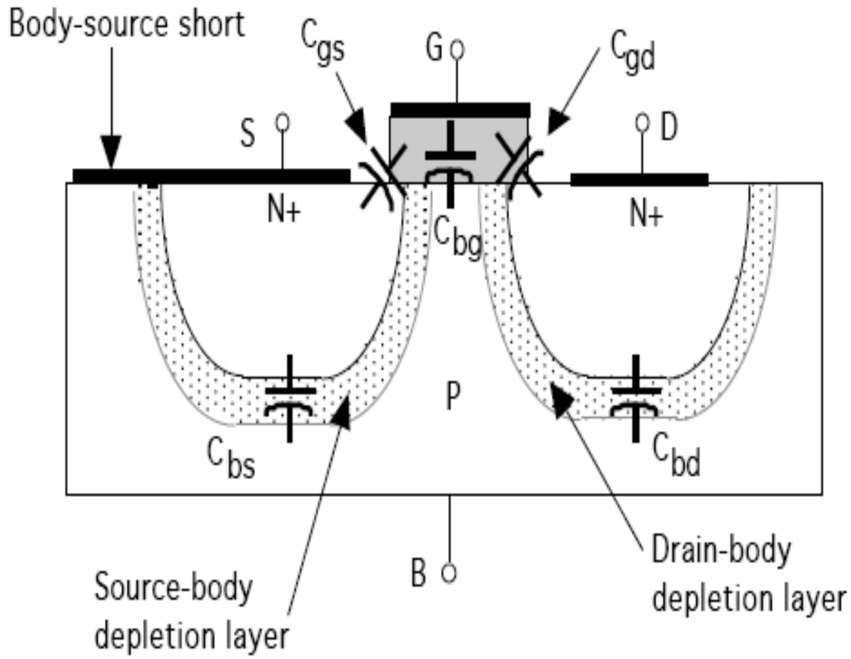
PSPICE Built-in MOSFET Model



Circuit components

- RG, RDS, RS, RB, and RD = parasitic ohmic resistances
- Cgs Cgd, and Cgb = constant voltage-independent capacitors
- Cbs and Cbd = nonlinear voltage-dependent capacitors (depletion layer capacitances)
- Idrain = f(Vgs, Vds) accounts for dc characteristics of MOSFET
- Model developed for lateral (signal level) MOSFETs

Lateral (Signal level) MOSFET



- C_{gs}, C_{bg}, C_{gd} due to electrostatic capacitance of gate oxide. Independent of applied voltage

- C_{bs} and C_{bd} due to depletion layers. Capacitance varies with junction voltage.

- Body-source short keeps C_{bs} constant.

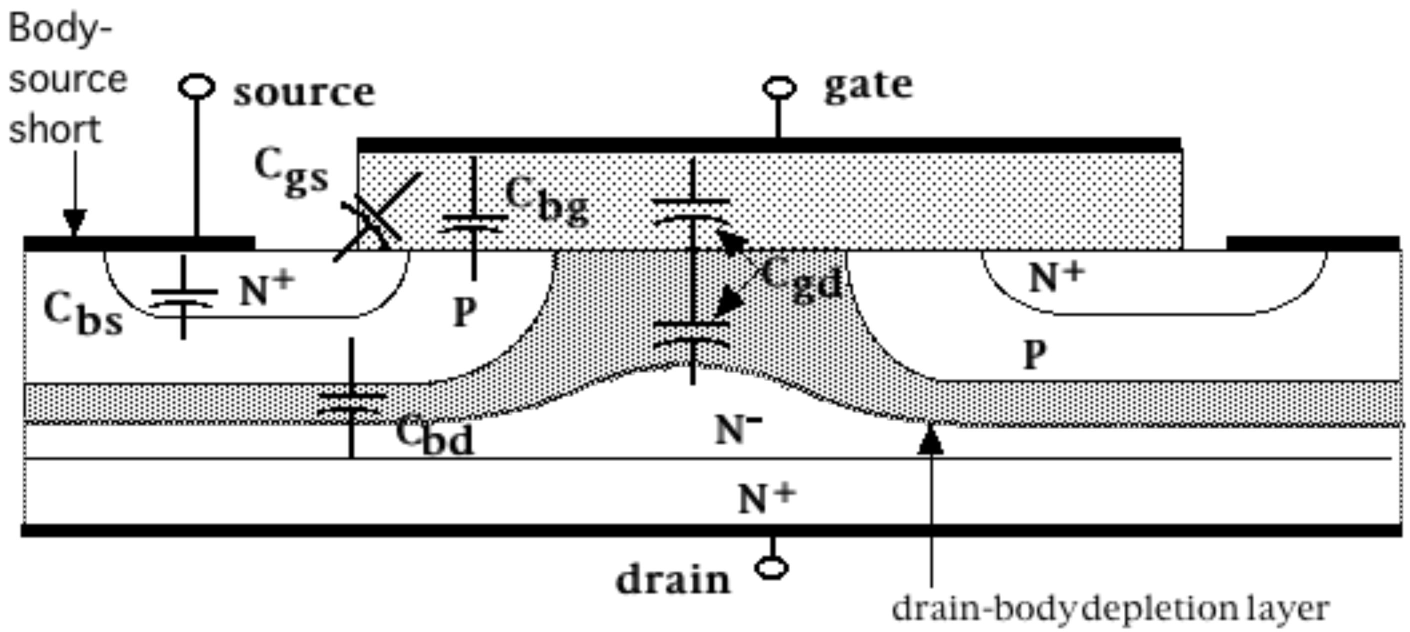
- Body-source short puts C_{bd} between drain and source.

- Variations in drain-source voltage relatively small, so changes in C_{bd} also relatively small.

- Capacitances relatively independent of terminal voltages

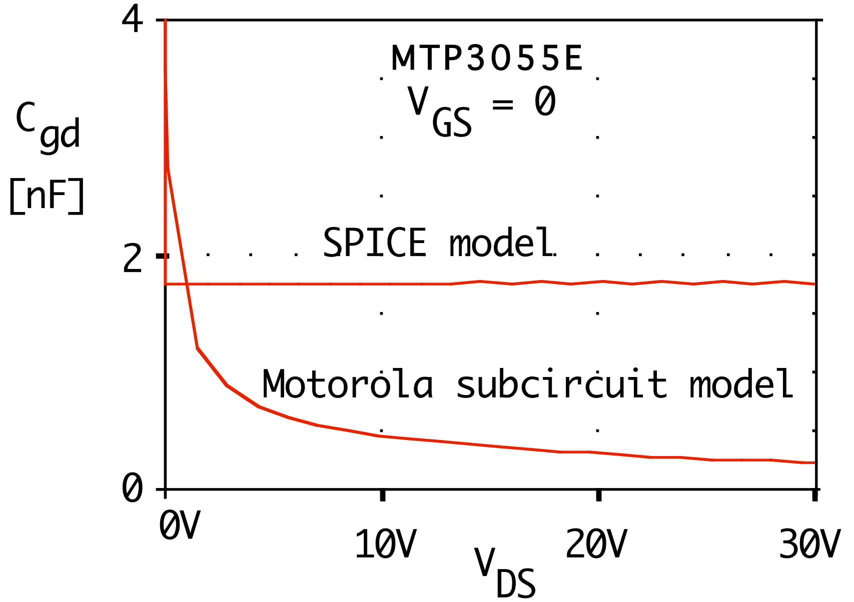
- Consequently PSPICE MOSFET model has voltage-independent capacitances.

Vertical Power MOSFET

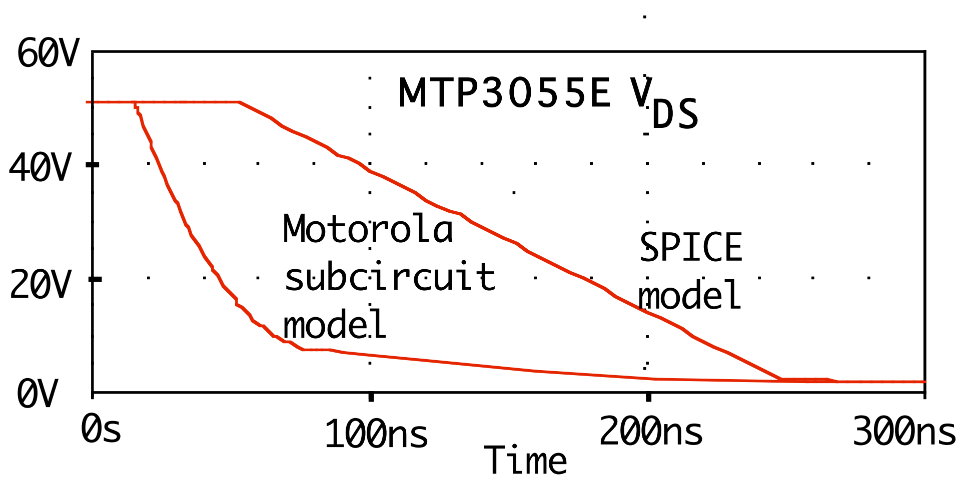


- Drain-drift region and large drain-source voltage variations cause large variations in drain-body depletion layer thickness
  - Large changes in C_{gd} with changes in drain-source voltage. 10 to 100:1 changes in C_{gd} measured in high voltage MOSFETs.
  - Moderate changes in C_{gb} and C_{bs}.
- MOSFET circuit simulation models must take this variation into account.

Inadequacies of PSPICE MOSFET Model

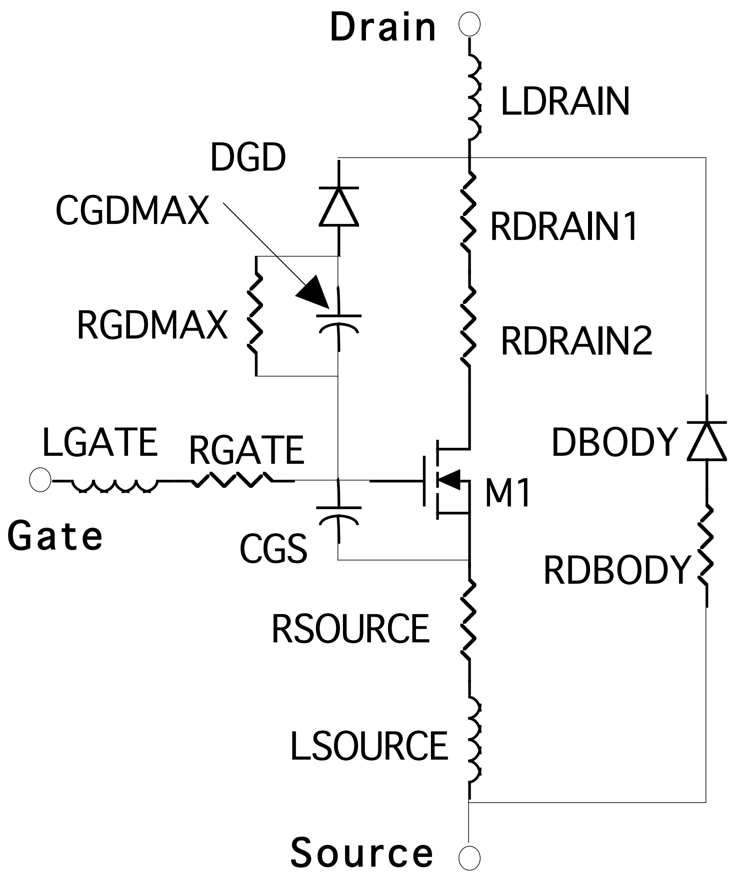


- C_{gs} and C_{gd} in PSPICE model are constant independent of terminal voltages
- In vertical power MOSFETs, C_{gd} varies substantially with terminal voltages.



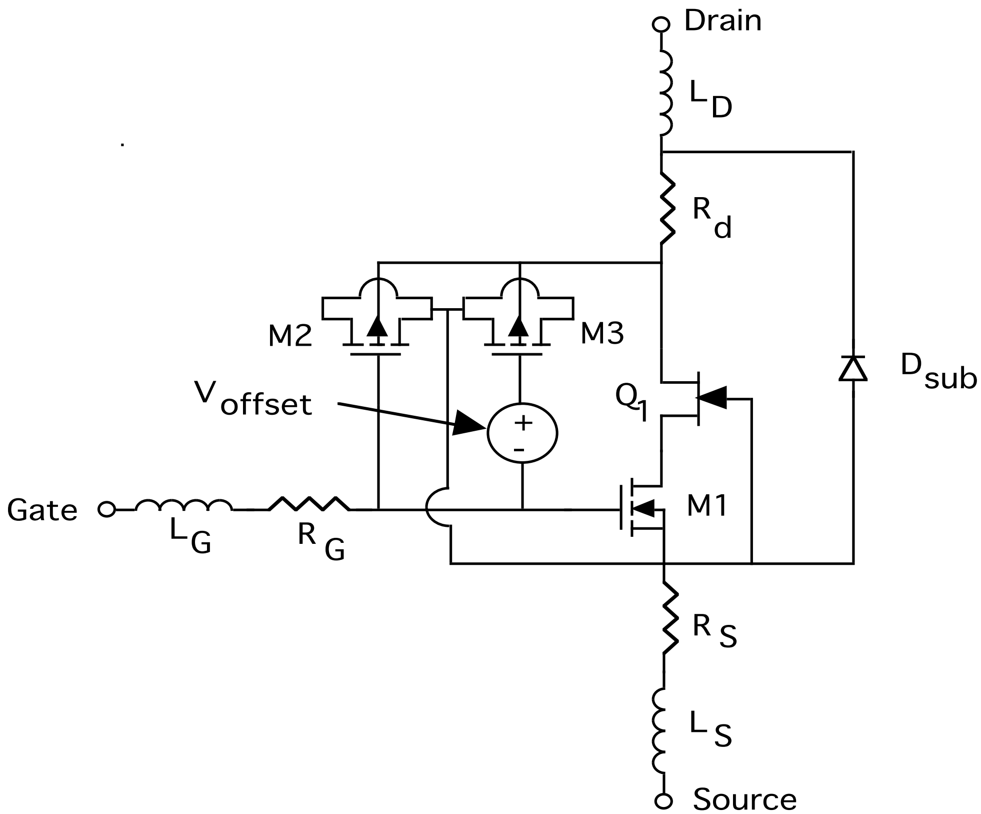
- Comparison of transient response of drain-source voltage using PSPICE model and an improved subcircuit model. Both models used in same step-down converter circuit.

Example of an Improved MOSFET Model



- Developed by Motorola for their TMOS line of power MOSFETs
- M1 uses built-in PSPICE models to describe dc MOSFET characteristics. Space charge capacitances of intrinsic model set to zero.
- Space charge capacitance of DGD models voltage-dependent gate-drain capacitance.
- CGDMAX insures that gate-drain capacitance does not get unrealistically large at very low drain voltages.
- DBODY models built-in anti-parallel diode inherent in the MOSFET structure.
- CGS models gate-source capacitance of MOSFET. Voltage dependence of this capacitance ignored in this model.
- Resistances and inductances model parasitic components due to packaging.
- Many other models described in literature. Too numerous to list here.

Another Improved MOSFET Simulation Model



- L_G, R_G, L_S R_S, L_D, R_D - parasitic inductances and resistances
- M1= intrinsic SPICE level 2 MOSFET with no parasitic resistances or capacitances.
- M2 and M3 are SPICE level 2 MOSFETs used along with V_{offset} to model voltage dependent behavior of C_{gd}.
- JFET Q_1 and R_d account for voltage drop in N^- drain drift region
- D_{sub} is built-in SPICE diode model used to account for parasitic anti-parallel diode in MOSFET structure.
- Reference - "An Accurate Model for Power DMOSFETs Including Inter-electrode Capacitances", Robert Scott, Gerhard A. Frantz, and Jennifer L. Johnson, IEEE Trans. on Power Electronics, Vol. 6, No. 2, pp. 192-198, (April, 1991)