POWER MOSFETS

INTRODUCTION TO FET'S

FET's use field effect for their operation. FET is manufactured by diffusing two areas of p-type into the n-type semiconductor as shown. Each p-region is connected to a gate terminal; the gate is a p-region while source and drain are n-region. Since it is similar to two diodes one is a gate source diode and the other is a gate drain diode.

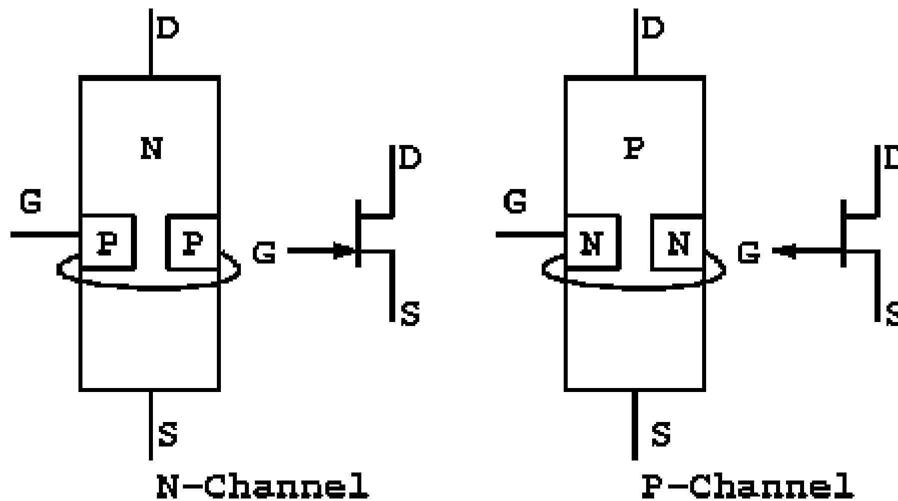

Fig:1: Schematic symbol of JFET

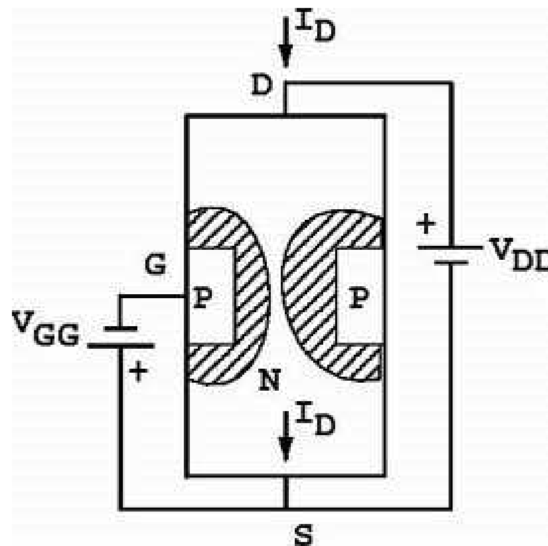

Fig. 2: Structure of FET with biasing

In BJT's we forward bias the B-E diode but in a JFET, we always reverse bias the gate-source diode. Since only a small reverse current can exist in the gate lead. Therefore $I_G = 0$, therefore $R_{in} = \infty(ideal)$.

The term field effect is related to the depletion layers around each p-region as shown. When the supply voltage V_{DD} is applied as shown it forces free electrons to flow

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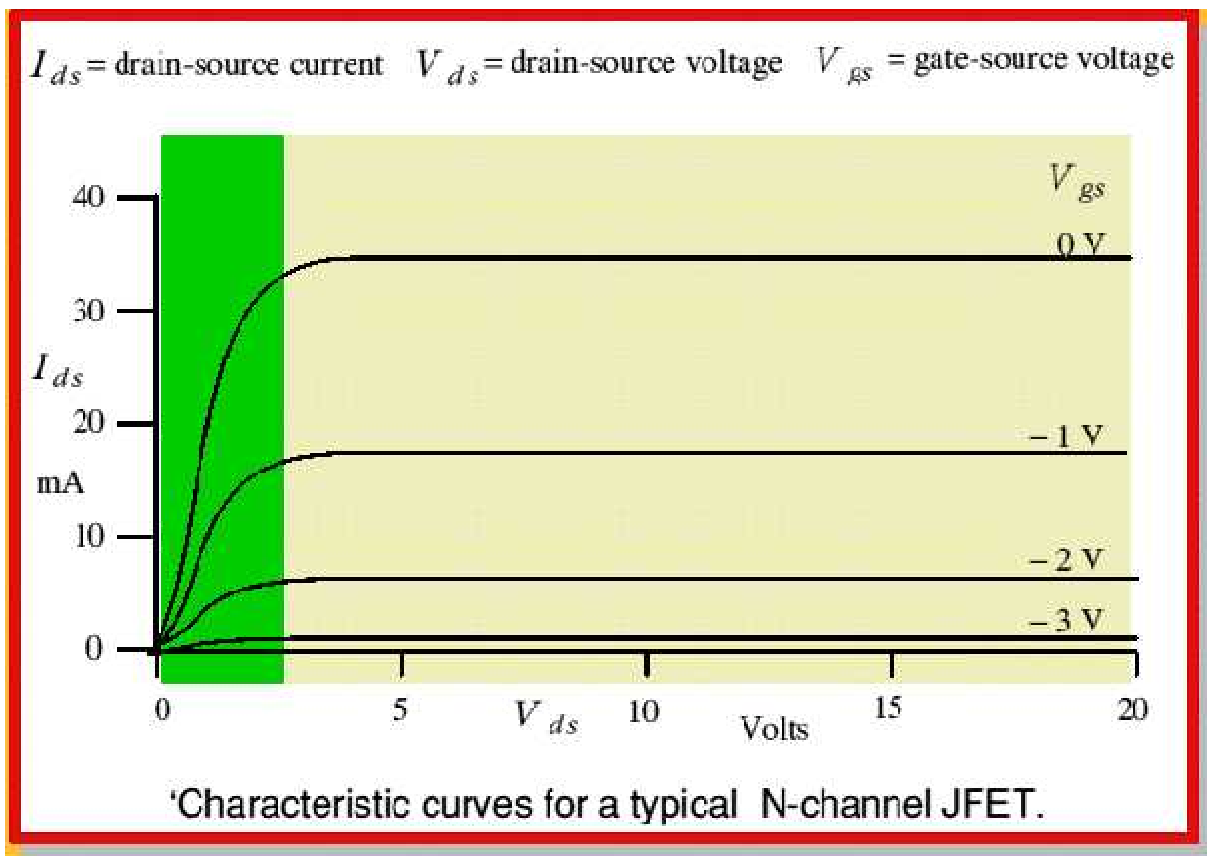
from source to drain. With gate reverse biased, the electrons need to flow from source to drain, they must pass through the narrow channel between the two depletion layers. The more the negative gate voltage is the tighter the channel becomes.

Therefore JFET acts as a voltage controlled device rather than a current controlled device.

JFET has almost infinite input impedance but the price paid for this is loss of control over the output current, since JFET is less sensitive to changes in the output voltage than a BJT.

JFET CHARACTERISTICS



'Characteristic curves for a typical N-channel JFET.

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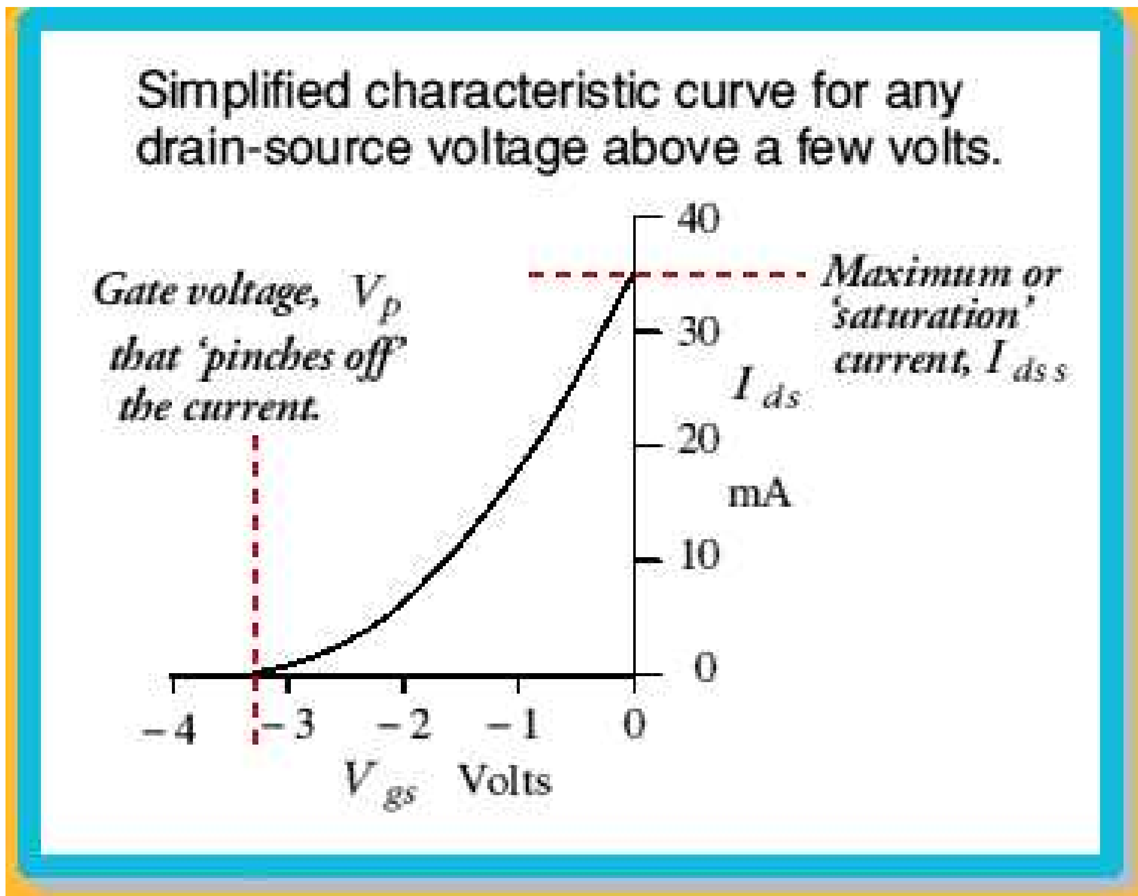

The maximum drain current out of a JFET occurs when $V_{GS} = 0$. As V_{DS} is increased for 0 to a few volts, the current will increase as determined by ohms law. As V_{DS} approaches V_P the depletion region will widen, carrying a noticeable reduction in channel width. If V_{DS} is increased to a level where the two depletion region would touch a pinch-off will result. I_D now maintains a saturation level I_{DSS}. Between 0 volts and pinch off voltage V_P is the ohmic region. After V_P, the regions constant current or active region.

If negative voltage is applied between gate and source the depletion region similar to those obtained with $V_{GS} = 0$ are formed but at lower values of V_{DS}. Therefore saturation level is reached earlier.

We can find two important parameters from the above characteristics

- r_{ds} = drain to source resistance = $\frac{\Delta V_{DS}}{\Delta I_D}$.
- g_m = transconductance of the device = $\frac{\Delta I_D}{\Delta V_{GS}}$.
- The gain of the device, amplification factor $\sim = r_{ds} g_m$.

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SHOCKLEY EQUATION

The FET is a square law device and the drain current I_D is given by the Shockley equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

and $$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

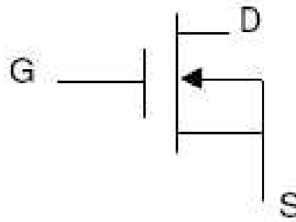
MOSFET

MOSFET stands for metal oxide semiconductor field effect transistor. There are two types of MOSFET

- Depletion type MOSFET
- Enhancement type MOSFET

DEPLETION TYPE MOSFET

CONSTRUCTION



Symbol of n-channel depletion type MOSFET

It consists of a highly doped p-type substrate into which two blocks of heavily doped n-type material are diffused to form a source and drain. A n-channel is formed by diffusing between source and drain. A thin layer of SiO_2 is grown over the entire surface and holes are cut in SiO_2 to make contact with n-type blocks. The gate is also connected to a metal contact surface but remains insulated from the n-channel by the SiO_2 layer. SiO_2 layer results in an extremely high input impedance of the order of 10^{10} to $10^{15}\Omega$ for this area.

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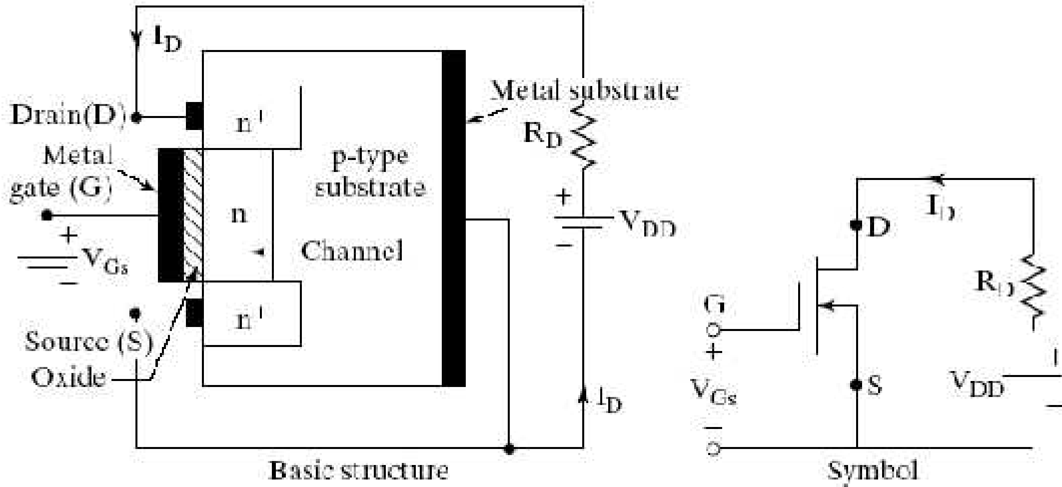


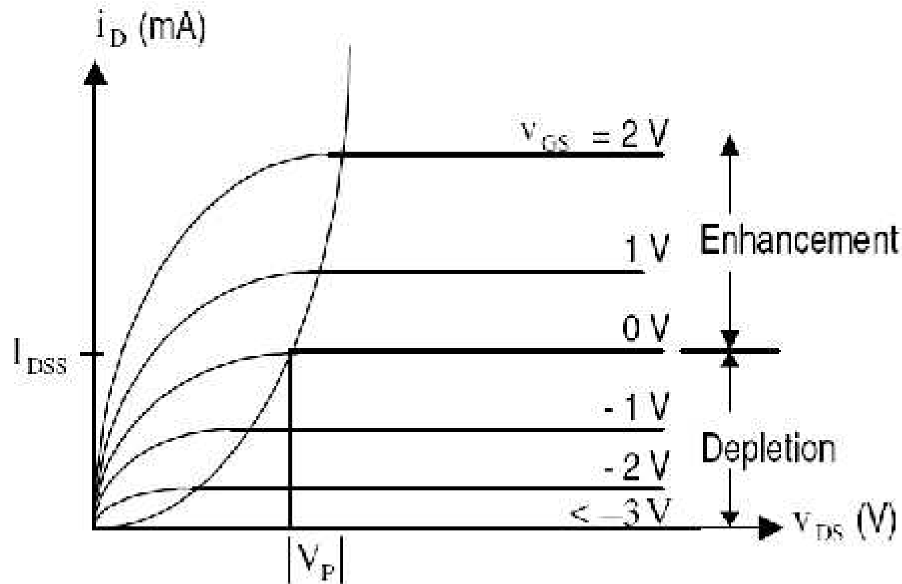
Fig. 4: Structure of n-channel depletion type MOSFET

OPERATION

When $V_{GS} = 0V$ and V_{DS} is applied and current flows from drain to source similar to JFET. When $V_{GS} = -1V$, the negative potential will tend to pressure electrons towards the p-type substrate and attracts hole from p-type substrate. Therefore recombination occurs and will reduce the number of free electrons in the n-channel for conduction. Therefore with increased negative gate voltage I_D reduces.

For positive values, V_{gs}, additional electrons from p-substrate will flow into the channel and establish new carriers which will result in an increase in drain current with positive gate voltage.

DRAIN CHARACTERISTICS



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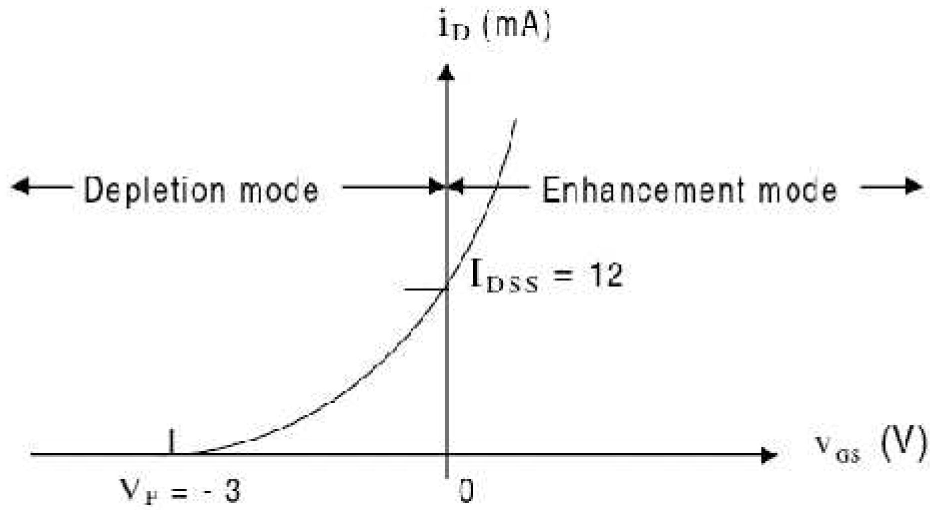
TRANSFER CHARACTERISTICS



ENHANCEMENT TYPE MOSFET

Here current control in an n-channel device is now affected by positive gate to source voltage rather than the range of negative voltages of JFET's and depletion type MOSFET.

BASIC CONSTRUCTION

A slab of p-type material is formed and two n-regions are formed in the substrate. The source and drain terminals are connected through metallic contacts to n-doped regions, but the absence of a channel between the doped n-regions. The SiO_2 layer is still present to isolate the gate metallic platform from the region between drain and source, but now it is separated by a section of p-type material.

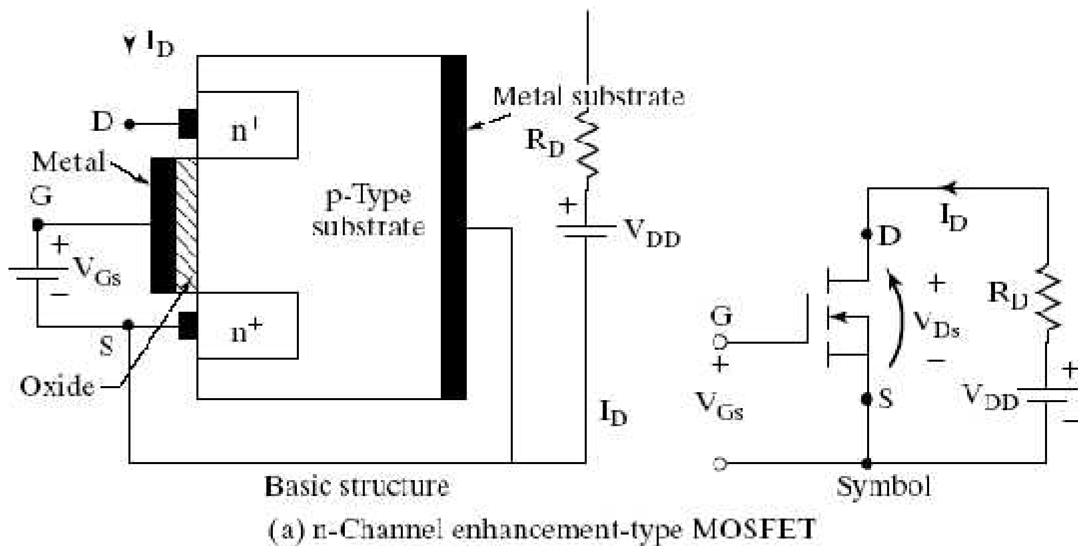


Fig. 5: Structure of n-channel enhancement type MOSFET

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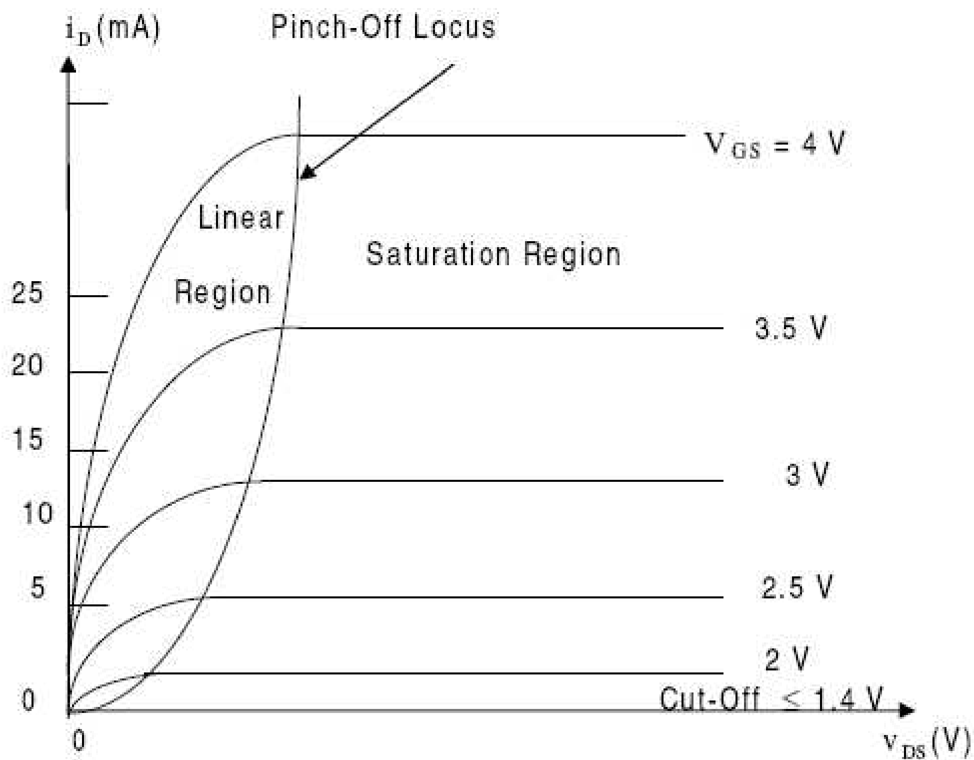
OPERATION

If $V_{GS} = 0V$ and a voltage is applied between the drain and source, the absence of a n-channel will result in a current of effectively zero amperes. With V_{DS} set at some positive voltage and V_{GS} set at 0V, there are two reverse biased p-n junction between the n-doped regions and p substrate to oppose any significant flow between drain and source.

If both V_{DS} and V_{GS} have been set at some positive voltage, then positive potential at the gate will pressure the holes in the p-substrate along the edge of SiO_2 layer to leave the area and enter deeper region of p-substrate. However the electrons in the p-substrate will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. The negative carriers will not be absorbed due to insulating SiO_2 layer, forming an inversion layer which results in current flow from drain to source.

The level of V_{GS} that results in significant increase in drain current is called threshold voltage V_T. As V_{GS} increases the density of free carriers will increase resulting in increased level of drain current. If V_{GS} is constant V_{DS} is increased; the drain current will eventually reach a saturation level as occurred in JFET.

DRAIN CHARACTERISTICS



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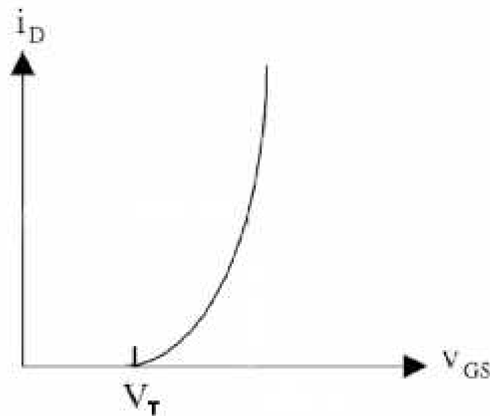
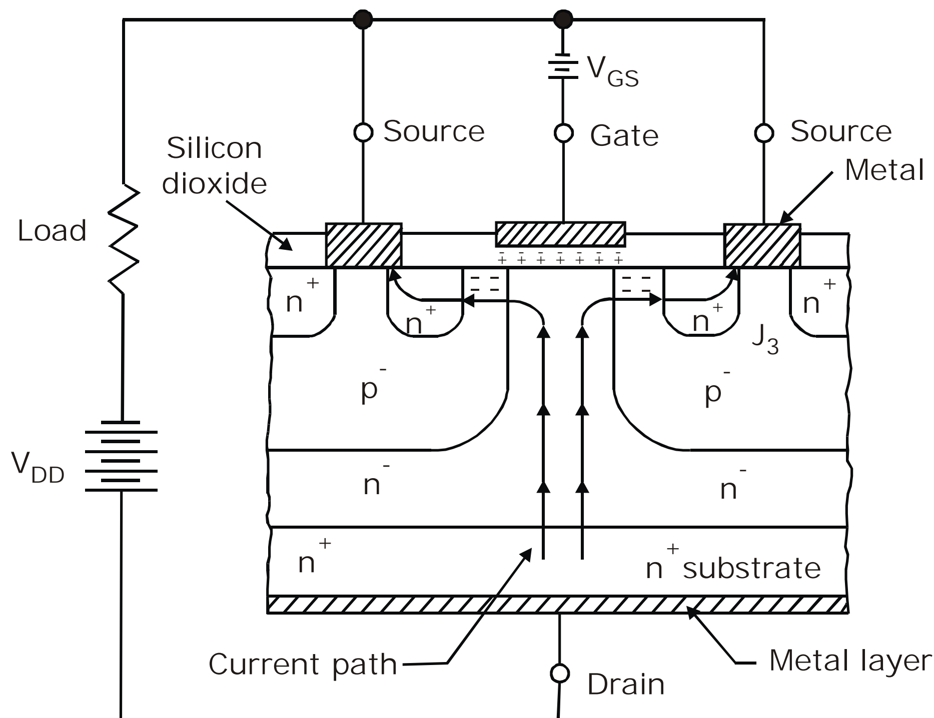
TRANSFER CHARACTERISTICS



POWER MOSFET'S

Power MOSFET's are generally of enhancement type only. This MOSFET is turned 'ON' when a voltage is applied between gate and source. The MOSFET can be turned 'OFF' by removing the gate to source voltage. Thus gate has control over the conduction of the MOSFET. The turn-on and turn-off times of MOSFET's are very small. Hence they operate at very high frequencies; hence MOSFET's are preferred in applications such as choppers and inverters. Since only voltage drive (gate-source) is required, the drive circuits of MOSFET are very simple. The paralleling of MOSFET's is easier due to their positive temperature coefficient. But MOSFTS's have high on-state resistance hence for higher currents; losses in the MOSFET's are substantially increased. Hence MOSFET's are used for low power applications.

CONSTRUCTION



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Power MOSFET's have additional features to handle larger powers. On the n^+ substrate high resistivity n^- layer is epitaxially grown. The thickness of n^- layer determines the voltage blocking capability of the device. On the other side of n^+ substrate, a metal layer is deposited to form the drain terminal. Now p^- regions are diffused in the epitaxially grown n^- layer. Further n^+ regions are diffused in the p^- regions as shown. SiO_2 layer is added, which is then etched so as to fit metallic source and gate terminals.

A power MOSFET actually consists of a parallel connection of thousands of basic MOSFET cells on the same single chip of silicon.

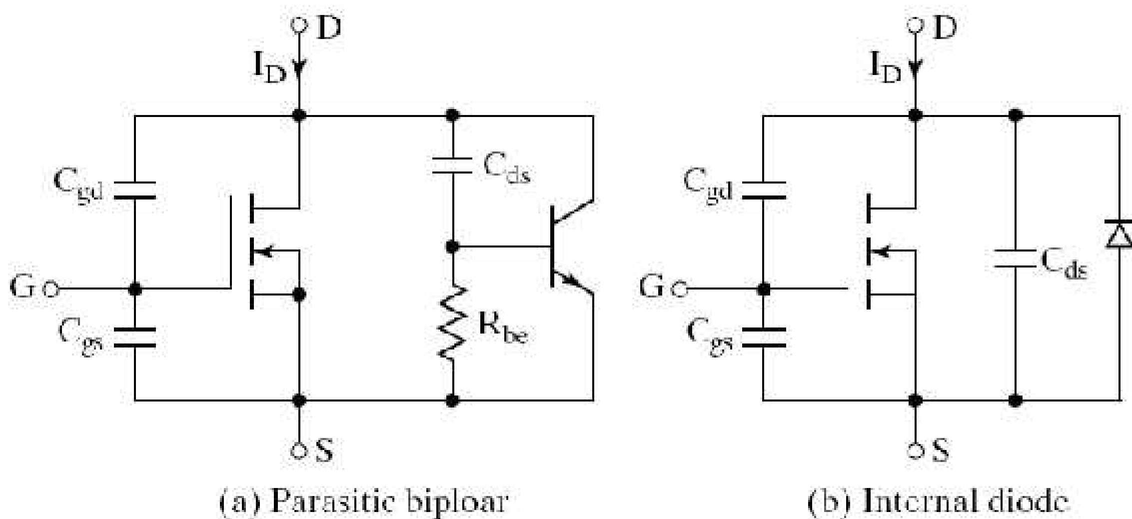
When gate circuit voltage is zero and V_{DD} is present, $n^+ - p^-$ junctions are reverse biased and no current flows from drain to source. When gate terminal is made positive with respect to source, an electric field is established and electrons from n^- channel in the p^- regions. Therefore a current from drain to source is established.

Power MOSFET conduction is due to majority carriers therefore time delays caused by removal of recombination of minority carriers is removed.

Because of the drift region the ON state drop of MOSFET increases. The thickness of the drift region determines the breakdown voltage of MOSFET. As seen a parasitic BJT is formed, since emitter base is shorted to source it does not conduct.

SWITCHING CHARACTERISTICS

The switching model of MOSFET's is as shown in the figure 6(a). The various inter electrode capacitance of the MOSFET which cannot be ignored during high frequency switching are represented by C_{gs}, C_{gd} & C_{ds}. The switching waveforms are as shown in figure 7 . The turn on time t_d is the time that is required to charge the input capacitance to the threshold voltage level. The rise time t_r is the gate charging time from this threshold level to the full gate voltage V_{gsp}. The turn off delay time t_{doff} is the time required for the input capacitance to discharge from overdriving the voltage V_1 to the pinch off region. The fall time is the time required for the input capacitance to discharge from pinch off region to the threshold voltage. Thus basically switching ON and OFF depend on the charging time of the input gate capacitance.



(a) Parasitic biploar (b) Internal diode

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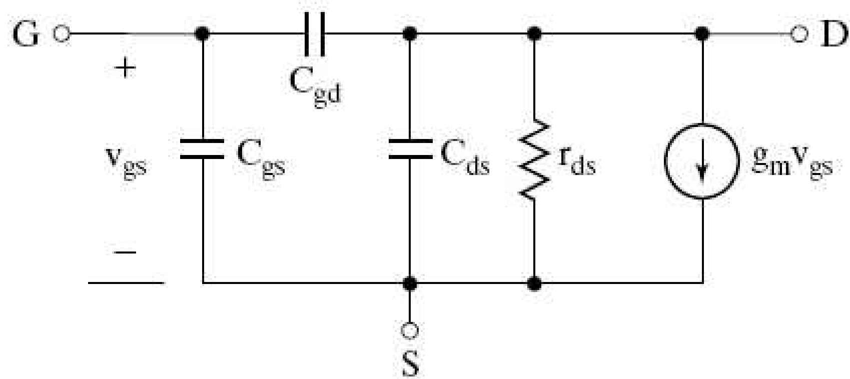

Fig.6: Switching model of MOSFET

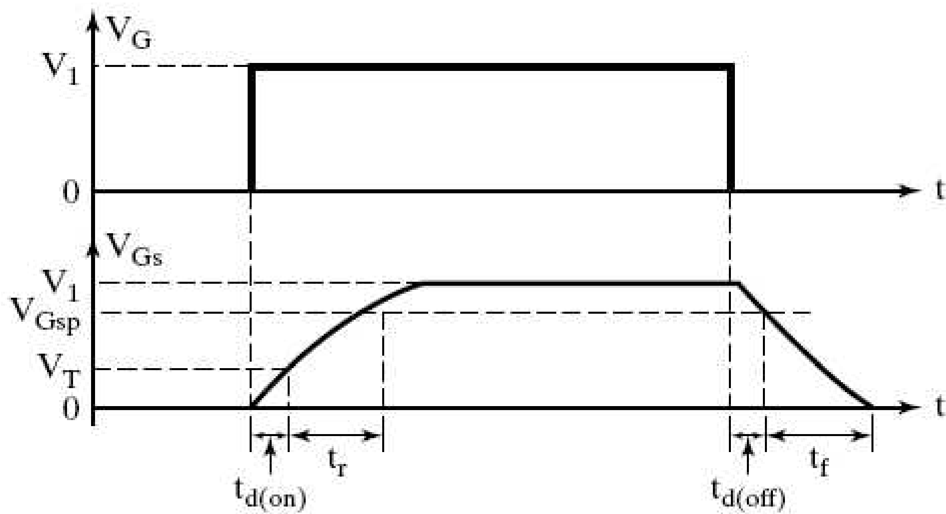

Fig.7: Switching waveforms and times of Power MOSFET

GATE DRIVE

The turn-on time can be reduced by connecting a RC circuit as shown to charge the capacitance faster. When the gate voltage is turned on, the initial charging current of the capacitance is

$$I_G = \frac{V_G}{R_S}.$$

The steady state value of gate voltage is

$$V_{GS} = \frac{R_G V_G}{R_S + R_1 + R_G}.$$

Where R_S is the internal resistance of gate drive force.

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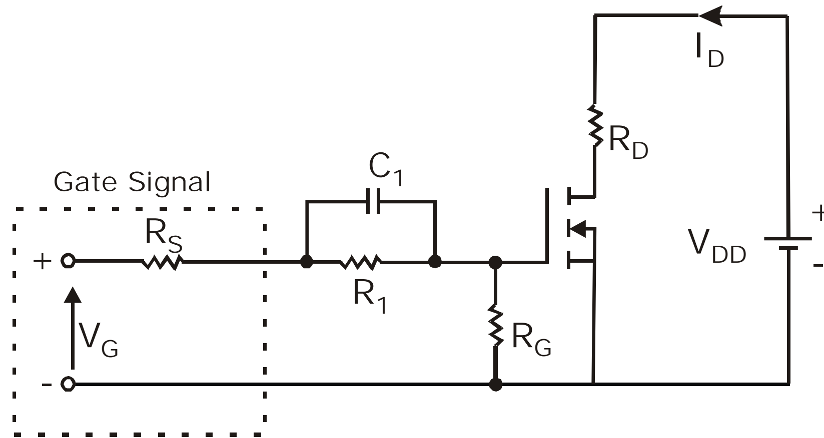

Fig. 8: Fast turn on gate drive circuit

COMPARISON OF MOSFET WITH BJT

- Power MOSFETS have lower switching losses but its on-resistance and conduction losses are more. A BJT has higher switching loss bit lower conduction loss. So at high frequency applications power MOSFET is the obvious choice. But at lower operating frequencies BJT is superior.
- MOSFET has positive temperature coefficient for resistance. This makes parallel operation of MOSFET's easy. If a MOSFET shares increased current initially, it heats up faster, its resistance increases and this increased resistance causes this current to shift to other devices in parallel. A BJT is a negative temperature coefficient, so current shaving resistors are necessary during parallel operation of BJT's.
- In MOSFET secondary breakdown does not occur because it have positive temperature coefficient. But BJT exhibits negative temperature coefficient which results in secondary breakdown.
- Power MOSFET's in higher voltage ratings have more conduction losses.
- Power MOSFET's have lower ratings compared to BJT's . Power MOSFET's → 500V to 140A, BJT → 1200V, 800A.

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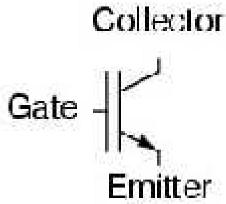
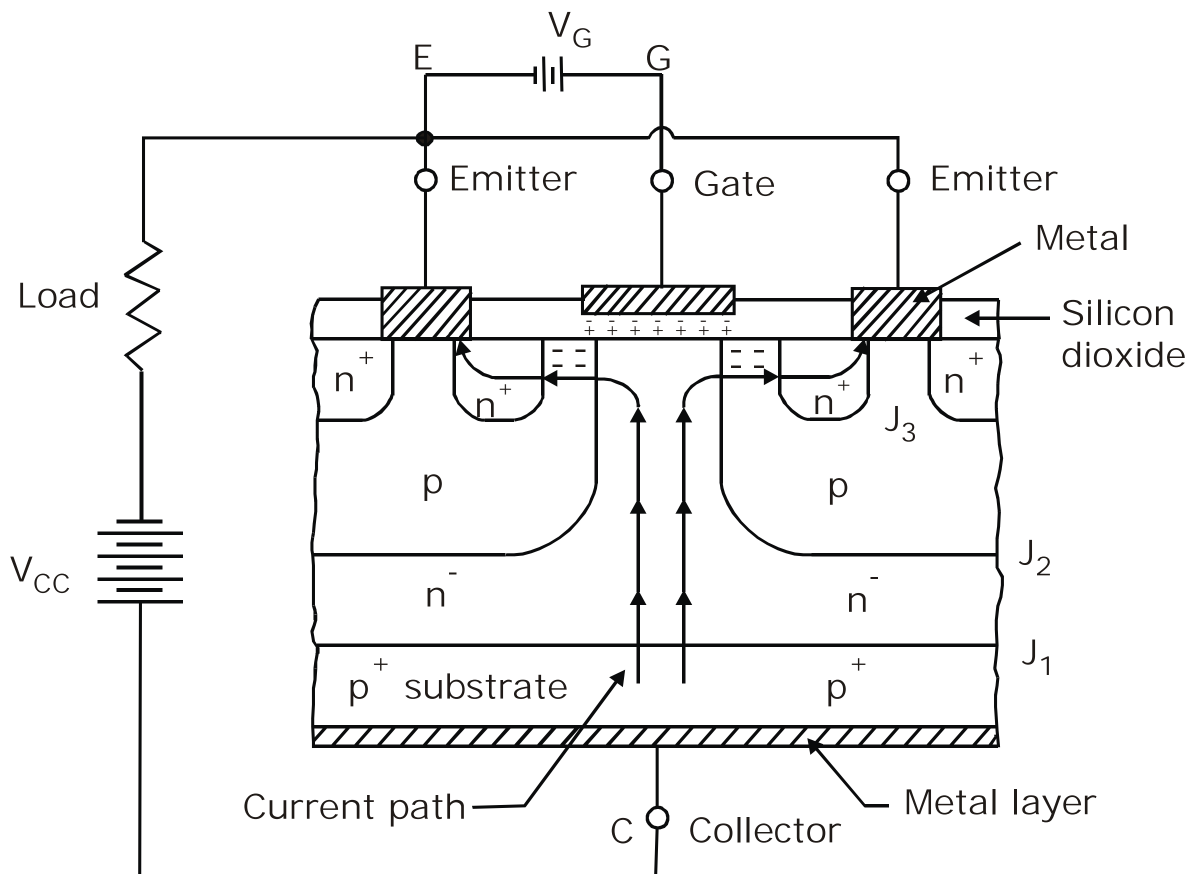
MOSIGT OR IGBT



The metal oxide semiconductor insulated gate transistor or IGBT combines the advantages of BJT's and MOSFET's. Therefore an IGBT has high input impedance like a MOSFET and low-on state power loss as in a BJT. Further IGBT is free from second breakdown problem present in BJT.

IGBT BASIC STRUCTURE AND WORKING



It is constructed virtually in the same manner as a power MOSFET. However, the substrate is now a p^+ layer called the collector.

When gate is positive with respect to positive with respect to emitter and with gate emitter voltage greater than V_{GSTH}, an n channel is formed as in case of power MOSFET. This n^- channel short circuits the n^- region with n^+ emitter regions.

An electron movement in the n^- channel in turn causes substantial hole injection from p^+ substrate layer into the epitaxially n^- layer. Eventually a forward current is established.

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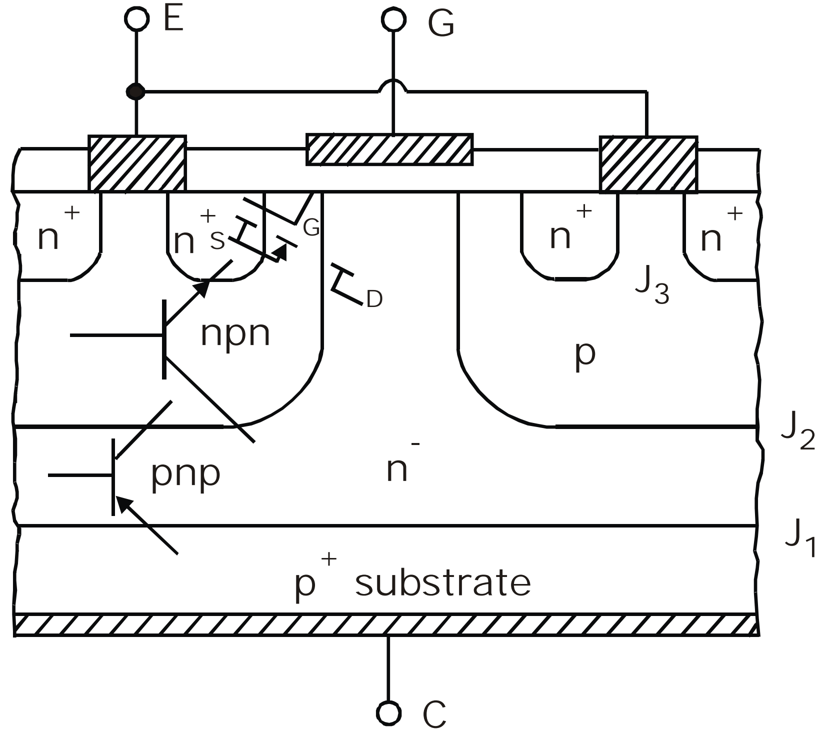
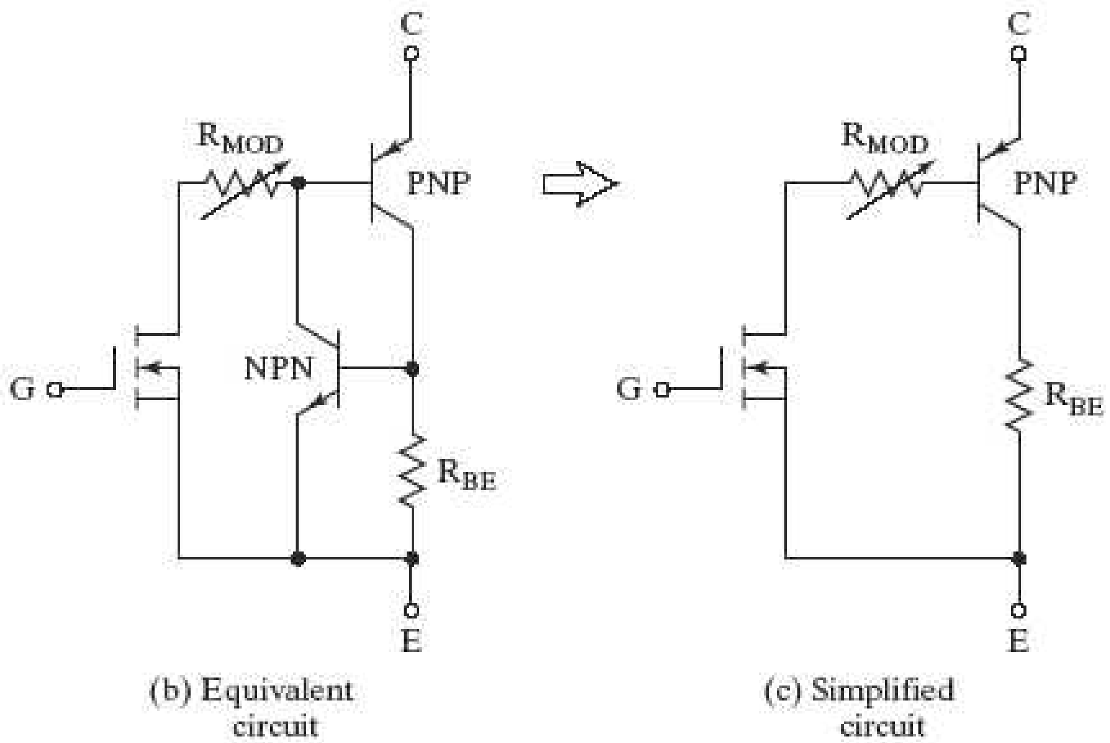
The three layers p^+, n^- and p constitute a pnp transistor with p^+ as emitter, n^- as base and p as collector. Also n^- , p and n^+ layers constitute a npn transistor. The MOSFET is formed with input gate, emitter as source and n^- region as drain. Equivalent circuit is as shown below.





(b) Equivalent circuit

(c) Simplified circuit

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Also p serves as collector for pnp device and also as base for npn transistor. The two pnp and npn is formed as shown.

When gate is applied $\left(V_{GS} > V_{GSth}\right)$ MOSFET turns on. This gives the base drive to T_1. Therefore T_1 starts conducting. The collector of T_1 is base of T_2. Therefore regenerative action takes place and large number of carriers are injected into the n^- drift region. This reduces the ON-state loss of IGBT just like BJT.

When gate drive is removed IGBT is turn-off. When gate is removed the induced channel will vanish and internal MOSFET will turn-off. Therefore T_1 will turn-off it T_2 turns off.

Structure of IGBT is such that R_1 is very small. If R_1 small T_1 will not conduct therefore IGBT's are different from MOSFET's since resistance of drift region reduces when gate drive is applied due to p^+ injecting region. Therefore ON state IGBT is very small.

IGBT CHARACTERISTICS

STATIC CHARACTERISTICS

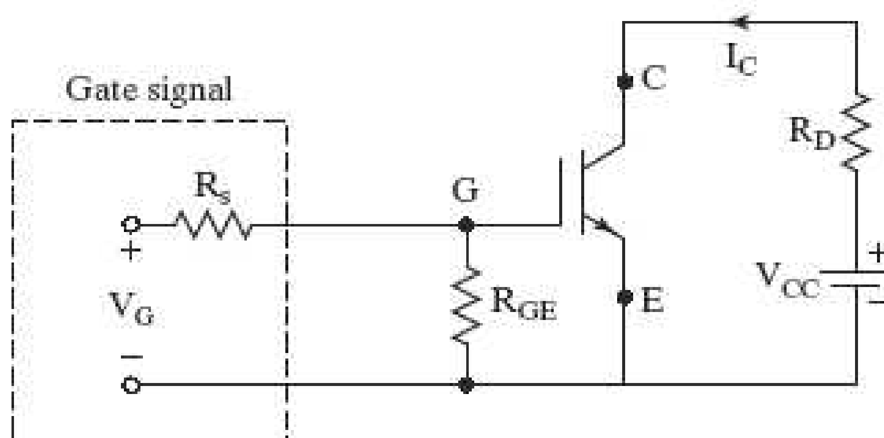

Fig. 9: IGBT bias circuit

Static V-I characteristics (I_C versus V_{CE})

Same as in BJT except control is by V_{GE}. Therefore IGBT is a voltage controlled device.

Transfer Characteristics (I_C versus V_{GE})

Identical to that of MOSFET. When $V_{GE} < V_{GET}$, IGBT is in off-state.

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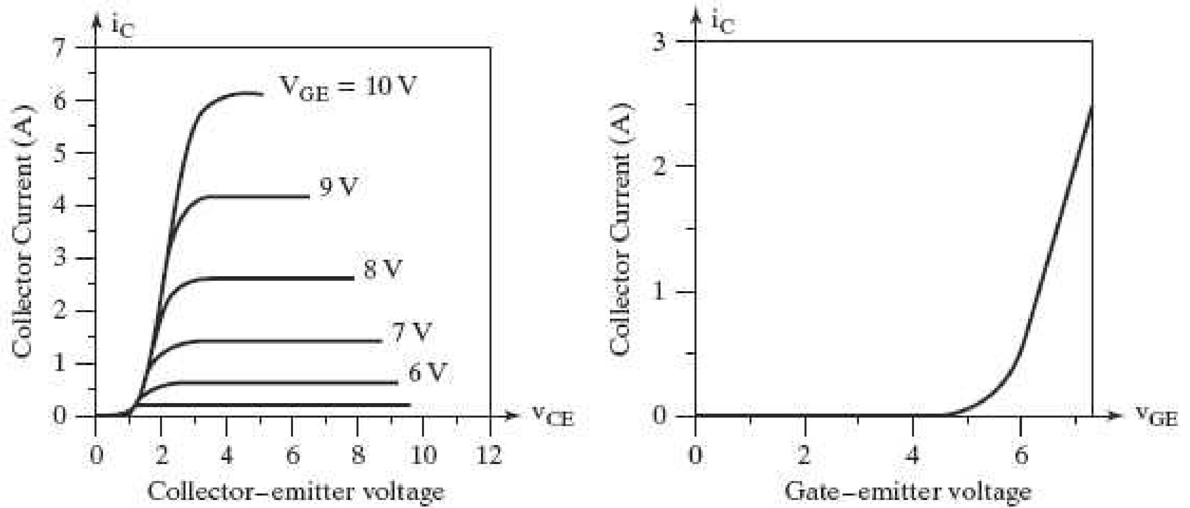

APPLICATIONS

Widely used in medium power applications such as DC and AC motor drives, UPS systems, Power supplies for solenoids, relays and contractors.

Though IGBT's are more expensive than BJT's, they have lower gate drive requirements, lower switching losses. The ratings up to 1200V, 500A.

SERIES AND PARALLEL OPERATION

Transistors may be operated in series to increase their voltage handling capability. It is very important that the series-connected transistors are turned on and off simultaneously. Other wise, the slowest device at turn-on and the fastest devices at turn-off will be subjected to the full voltage of the collector emitter circuit and the particular device may be destroyed due to high voltage. The devices should be matched for gain, transconductance, threshold voltage, on state voltage, turn-on time, and turn-off time. Even the gate or base drive characteristics should be identical.

Transistors are connected in parallel if one device cannot handle the load current demand. For equal current sharings, the transistors should be matched for gain, transconductance, saturation voltage, and turn-on time and turn-off time. But in practice, it is not always possible to meet these requirements. A reasonable amount of current sharing (45 to 55% with two transistors) can be obtained by connecting resistors in series with the emitter terminals as shown in the figure 10.

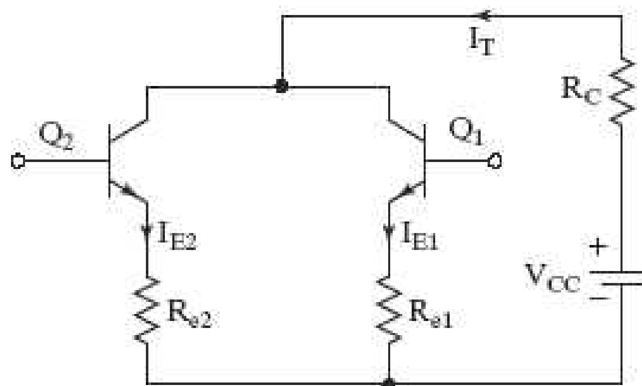

Fig. 10: Parallel connection of Transistors

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The resistor will help current sharing under steady state conditions. Current sharing under dynamic conditions can be accomplished by connecting coupled inductors. If the current through Q_1 rises, the $l(di/dt)$ across L_1 increases, and a corresponding voltage of opposite polarity is induced across inductor L_2. The result is low impedance path, and the current is shifted to Q_2. The inductors would generate voltage spikes and they may be expensive and bulky, especially at high currents.

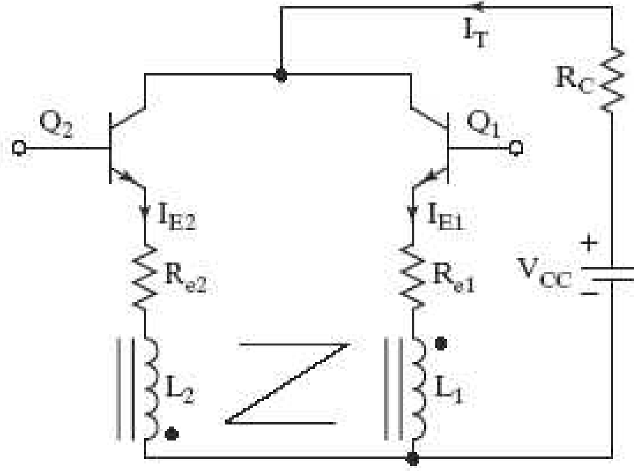

Fig. 11: Dynamic current sharing

BJTs have a negative temperature coefficient. During current sharing, if one BJT carries more current, its on-state resistance decreases and its current increases further, whereas MOSFETS have positive temperature coefficient and parallel operation is relatively easy. The MOSFET that initially draws higher current heats up faster and its on-state resistance increases, resulting in current shifting to the other devices. IGBTs require special care to match the characteristics due to the variations of the temperature coefficients with the collector current.

PROBLEM

1. Two MOSFETS which are connected in parallel carry a total current of $I_T = 20A$. The drain to source voltage of MOSFET M_1 is $V_{DS1} = 2.5V$ and that of MOSFET M_2 is $V_{DS2} = 3V$. Determine the drain current of each transistor and difference in current sharing it the current sharing series resistances are (a) $R_{s1} = 0.3\Omega$ and $R_{s2} = 0.2\Omega$, and (b) $R_{s1} = R_{s2} = 0.5\Omega$.

Solution

(a) $$I_{D1} + I_{D2} = I_T \ \& V_{DS1} + I_{D1}R_{s1} = V_{DS2} + I_{D2}R_{s2} = R_{s2}\left(I_T - I_D\right)$$

$$I_{D1} = \frac{V_{DS2} - V_{DS1} + I_T R_{s2}}{R_{s1} + R_{s2}}$$

$$I_{D1} = \frac{3 - 2.5 + 20 \times 0.2}{0.3 + 0.2} = 9A \quad or \quad 45\%$$

$$I_{D2} = 20 - 9 = 11A \quad or \quad 55\%$$

$$\Delta I = 55 - 45 = 10\%$$

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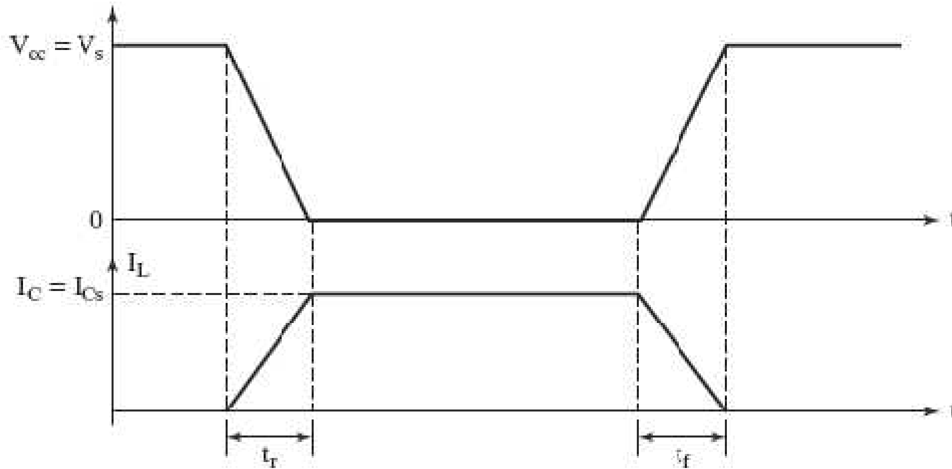
(b) $I_{D1} = \dfrac{3-2.5+20\times 0.5}{0.5+0.5} = 10.5A \quad or \quad 52.5\%$

$I_{D2} = 20-10.5 = 9.5A \quad or \quad 47.5\%$

$\Delta I = 52.5-47.5 = 5\%$

di/dt AND dv/dt LIMITATIONS

Transistors require certain turn-on and turn-off times. Neglecting the delay time t_d and the storage time t_s, the typical voltage and current waveforms of a BJT switch is shown below.



During turn-on, the collector rise and the di/dt is

$$\frac{di}{dt} = \frac{I_L}{t_r} = \frac{I_{cs}}{t_r} \quad ...(1)$$

During turn off, the collector emitter voltage must rise in relation to the fall of the collector current, and is

$$\frac{dv}{dt} = \frac{V_s}{t_f} = \frac{V_{cc}}{t_f} \quad ...(2)$$

The conditions di/dt and dv/dt in equation (1) and (2) are set by the transistor switching characteristics and must be satisfied during turn on and turn off. Protection circuits are normally required to keep the operating di/dt and dv/dt within the allowable limits of transistor. A typical switch with di/dt and dv/dt protection is shown in figure (a), with operating wave forms in figure (b). The RC network across the transistor is known as the snubber circuit or snubber and limits the dv/dt. The inductor L_S, which limits the di/dt, is sometimes called series snubber.

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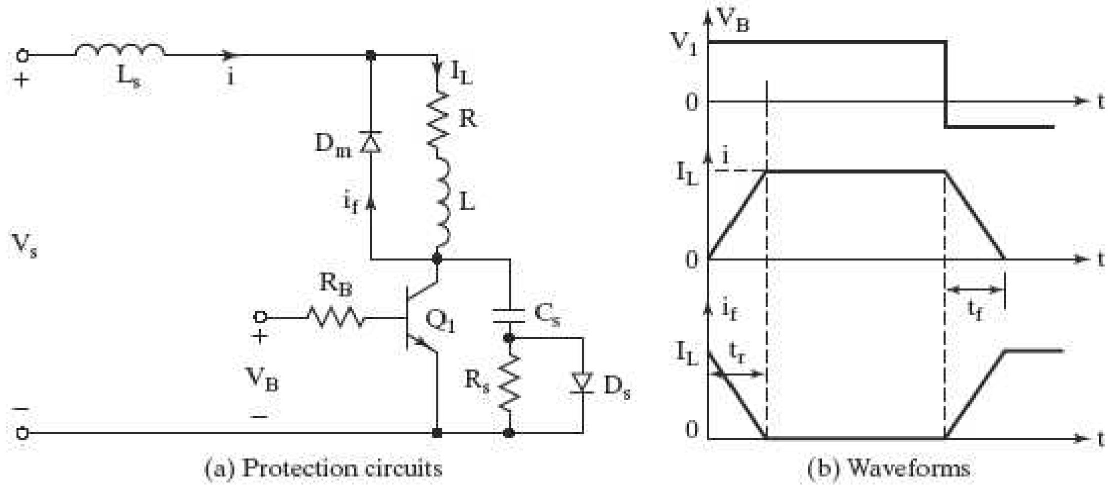
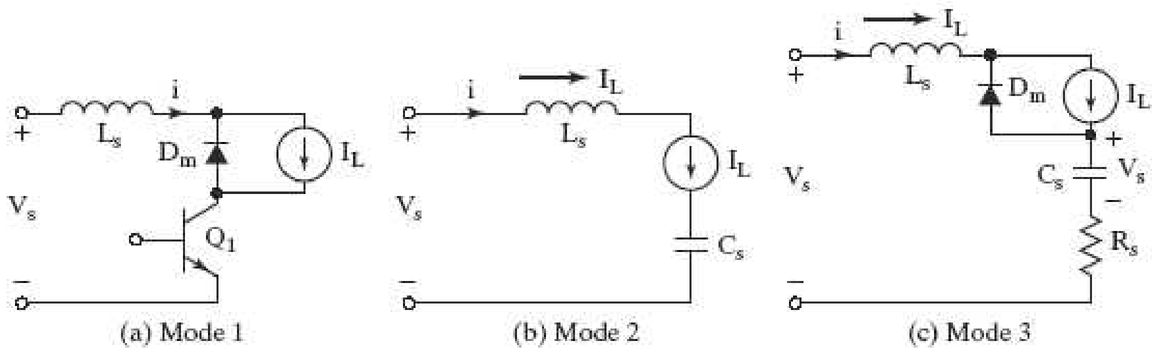


(a) Protection circuits (b) Waveforms

Let us assume that under steady state conditions the load current I_L is free wheeling through diode D_m, which has negligible reverse reco`very time. When transistor Q_1 is turned on, the collector current rises and current of diode D_m falls, because D_m will behave as short circuited. The equivalent circuit during turn on is shown in figure below



(a) Mode 1 (b) Mode 2 (c) Mode 3

The turn on di/dt is

$$\frac{di}{dt} = \frac{V_s}{L_s} \qquad ...(3)$$

Equating equations (1) and (3) gives the value of L_s

$$L_s = \frac{V_s t_r}{I_L} \qquad ...(4)$$

During turn off, the capacitor C_s will charge by the load current and the equivalent circuit is shown in figure (4). The capacitor voltage will appear across the transistor and the dv/dt is

$$\frac{dv}{dt} = \frac{I_L}{C_s} \qquad ...(5)$$

Equating equation (2) to equation (5) gives the required value of capacitance,

$$C_s = \frac{I_L t_f}{V_s} \qquad ...(6)$$

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Once the capacitor is charge to V_s, the freewheeling diode will turn on. Due to the energy stored in L_s, there will be damped resonant circuit as shown in figure (5). The RLC circuit is normally made critically damped to avoid oscillations. For unity critical damping, $\delta = 1$, and equation $\delta = \frac{\alpha}{\omega_0} = \frac{R}{2}\sqrt{\frac{C}{L}}$ yields

$$R_s = 2\sqrt{\frac{L_s}{C_s}}$$

The capacitor C_s has to discharge through the transistor and the increase the peak current rating of the transistor. The discharge through the transistor can be avoided by placing resistor R_s across C_s instead of placing R_s across D_s.

The discharge current is shown in figure below. When choosing the value of R_s, the discharge time, $R_s C_s = \tau_s$ should also be considered. A discharge time of one third the switching period, T_s is usually adequate.

$$3R_s C_s = T_s = \frac{1}{f_s}$$

$$R_s = \frac{1}{3 f_s C_s}$$

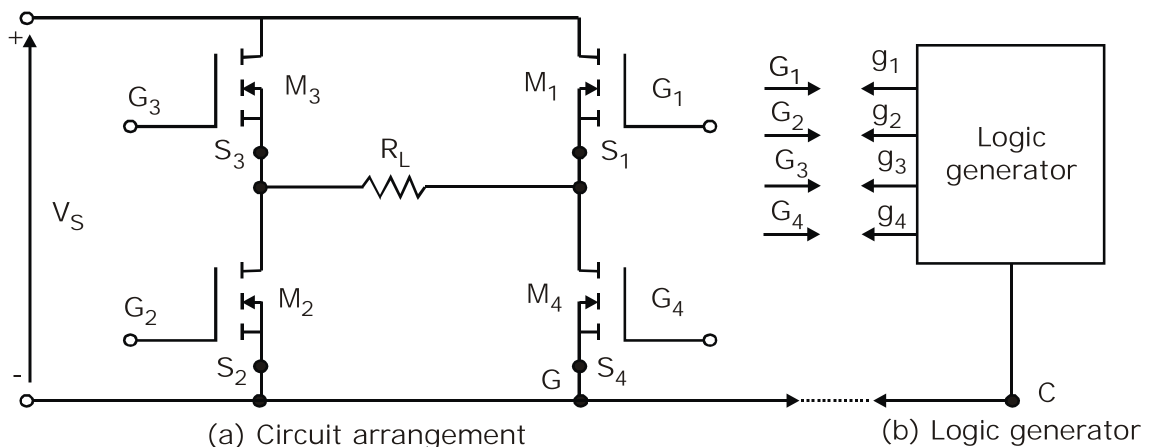
ISOLATION OF GATE AND BASE DRIVES

Necessity

Driver circuits are operated at very low power levels. Normally the gating circuit are digital in nature which means the signal levels are 3 to 12 volts. The gate and base drives are connected to power devices which operate at high power levels.

Illustration

The logic circuit generates four pulses; these pulses have common terminals. The terminal g, which has a voltage of V_G, with respect to terminal C, cannot be connected directly to gate terminal G, therefore V_{g1} should be applied between G_1 & S_1 of transistor Q_1. Therefore there is need for isolation between logic circuit and power transistor.



(a) Circuit arrangement (b) Logic generator

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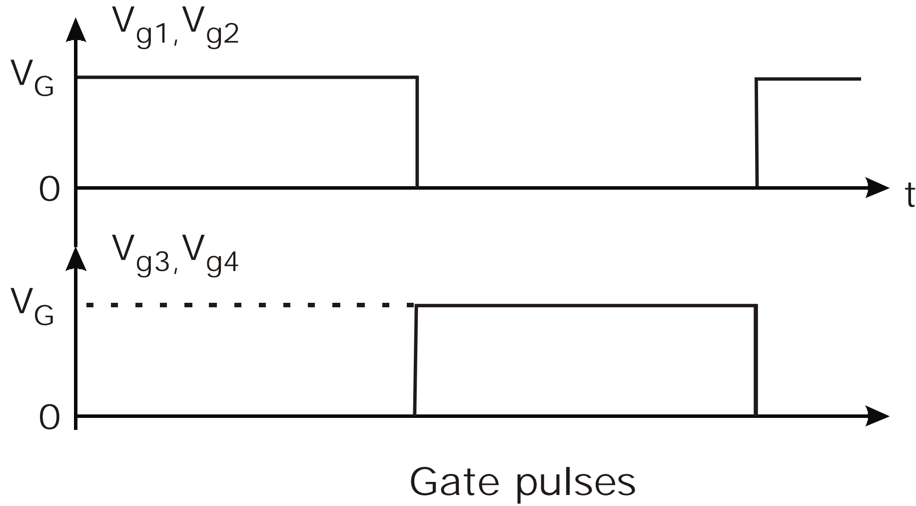
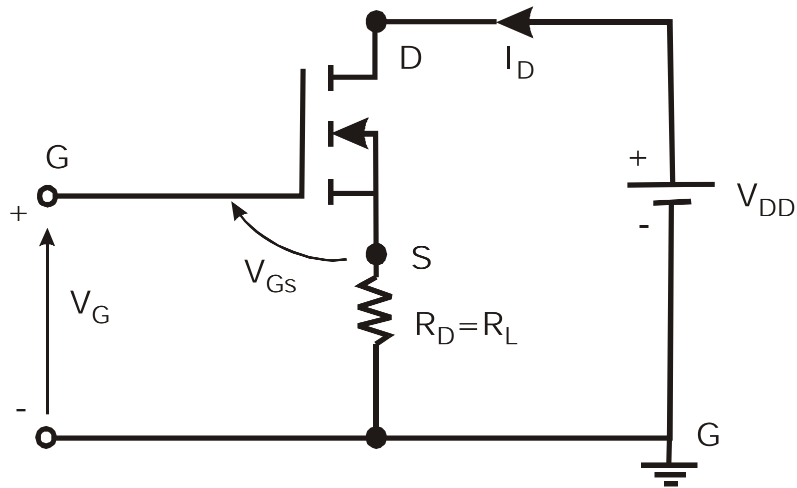


Gate pulses



There are two ways of floating or isolating control or gate signal with respect to ground.

- Pulse transformers
- Optocouplers

PULSE TRANSFORMERS

Pulse transformers have one primary winding and can have one or more secondary windings.

Multiple secondary windings allow simultaneous gating signals to series and parallel connected transistors. The transformer should have a very small leakage inductance and the rise time of output should be very small.

The transformer would saturate at low switching frequency and output would be distorted.

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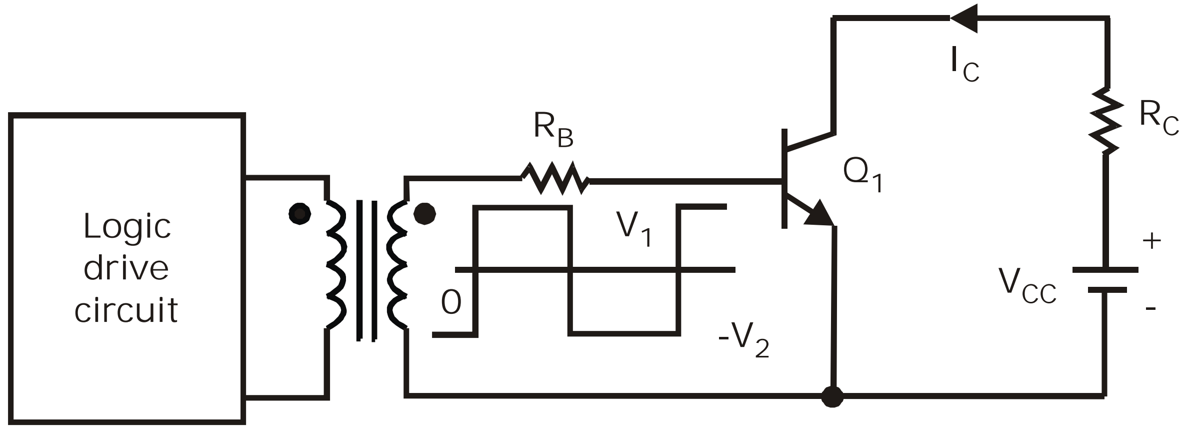
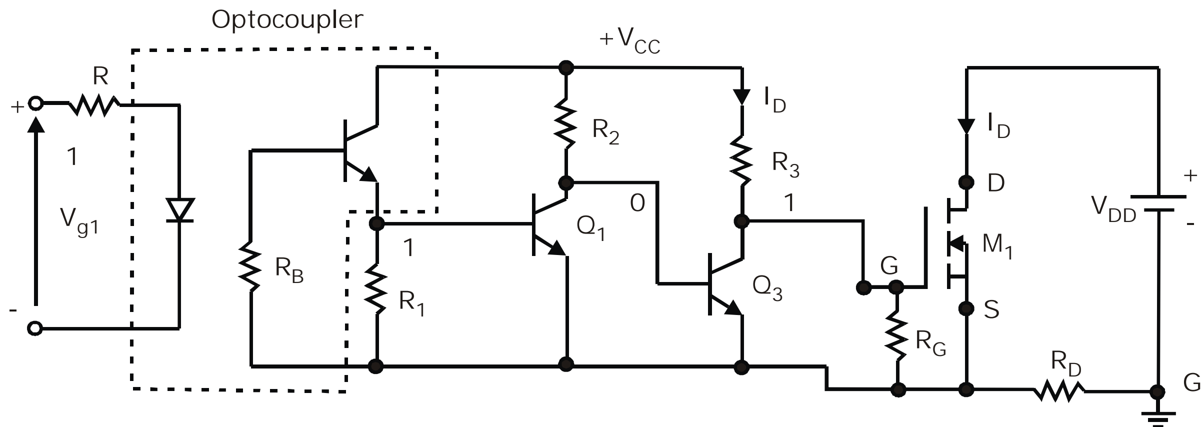


OPTOCOUPLERS

Optocouplers combine infrared LED and a silicon photo transistor. The input signal is applied to ILED and the output is taken from the photo transistor. The rise and fall times of photo transistor are very small with typical values of turn on time = $2.5 \sim s$ and turn off of 300ns. This limits the high frequency applications. The photo transistor could be a darlington pair. The phototransistor require separate power supply and add to complexity and cost and weight of driver circuits.



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